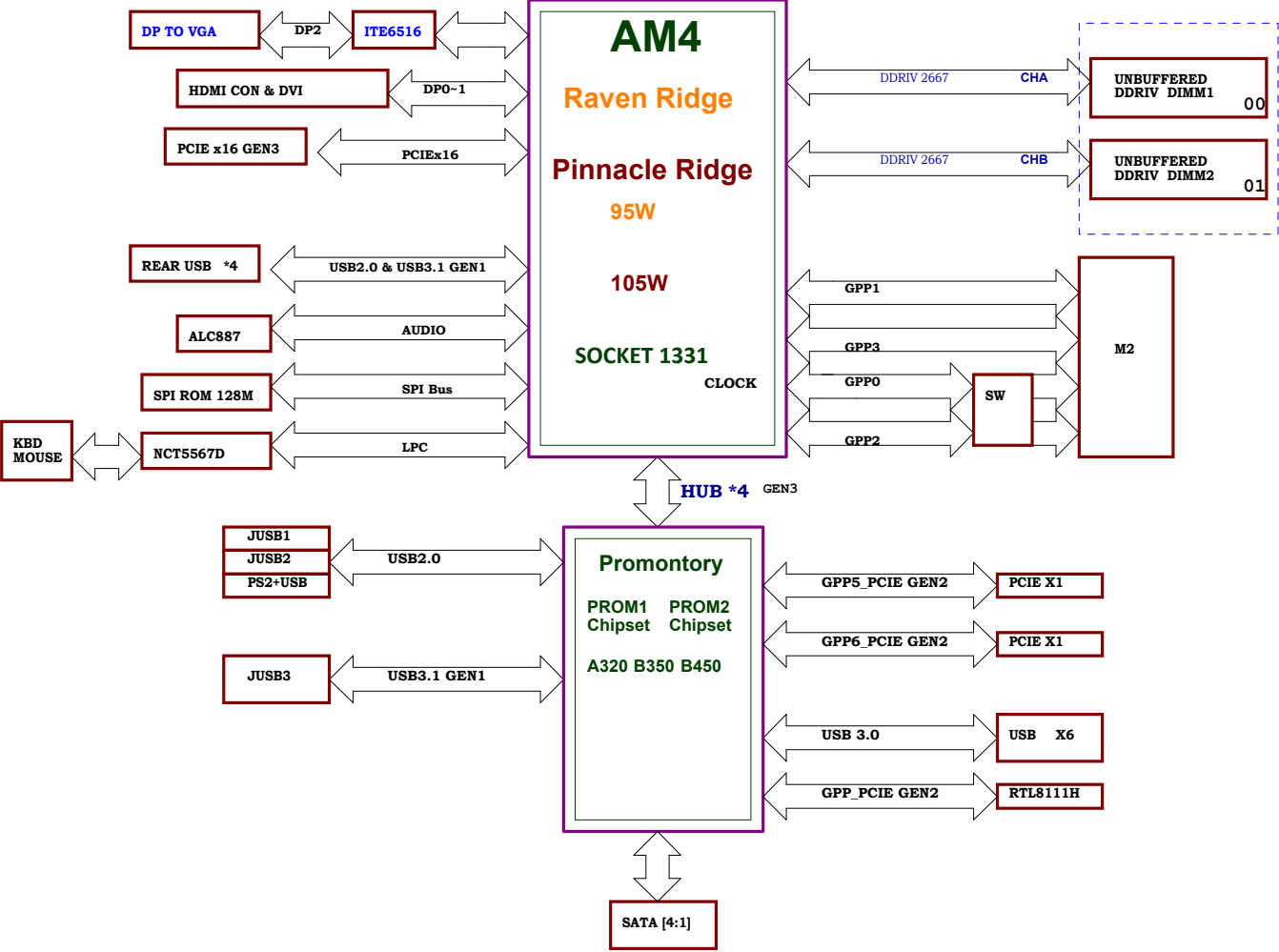


# MS-7B84 Ver:1.1

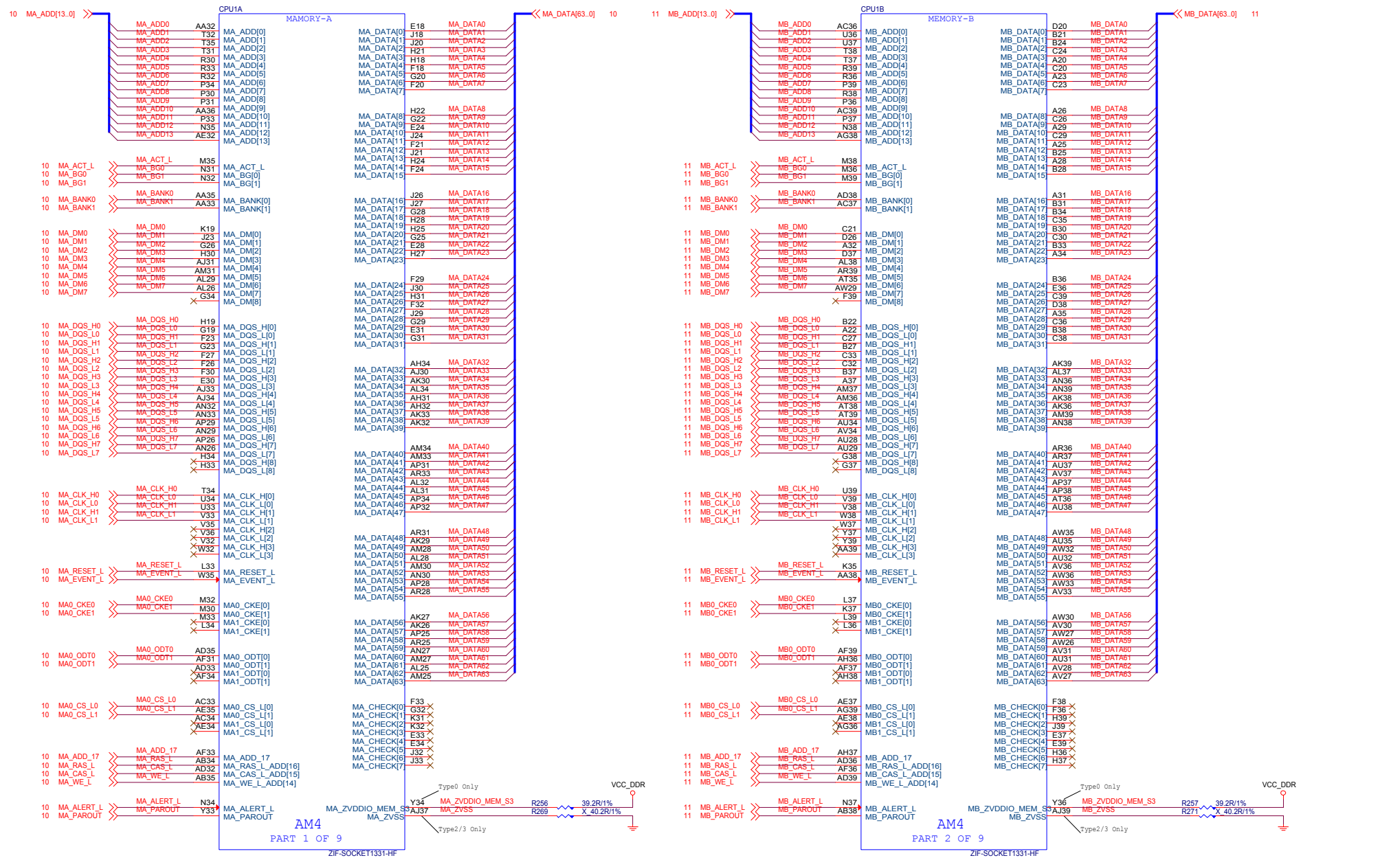
- CPU:**  
AMD AM4
- System Chipset:**  
Promontory A320 & B350 & B450  
(Value DIY or System Builder)
- Main Memory:**  
DDR IV \* 2 MAX:32 GB
- VRM**  
RT8894 4+2
- On Board Chipset:**  
LPC Super I/O --NCT5567  
LAN RTL8111H  
Azalia CODEC - Realtek ALC887
- Expansion Slots:**  
From CPU  
PCI Express X16 Slot \* 1  
PCI Express X1 Slot \* 1  
PCI Express X1 Slot \* 1  
M2\_2 \* 1
- OCF IC:**  
RT9553B

## FUSION BLOCK DIAGRAM



# AMD AM4

01 Block Diagram	37 CPU Power VDDP-MP8712
02 Cover Sheet	38 CPU Power Connector/PWRGD
03 FM4 DDR4 I/F	39 CPU Power RT8894 3+2 Phase
04 AM4 PCIE/SATAE	40/41 CPU Power Phase 1-4
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08 AM4 Power/RTC Power/ 09 AM4 GND	45 ATX/Front Panel
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14 Promontory-PCIE/SATA/SATAE	48 RTC Circuit/Moat Cap
15 Promontory-USB/OC	49 M2_2
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19 PCIE X16(X1*2) SLOT	52 Power Delivery
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21 DVI Connector	
22 CPU/SYS FAN Control TYPE K	
23 / 24 / 25 LAN-RTL8111H/Audio ALC887	
26 USB Rear PS2+USB2.0	
27 USB Rear LAN+USB3.1 GEN1	
28 USB Front Side	
29 SATA Connector	
30 HDMI Connector	
31 DP to VGA RTD2166	
32 ACPI uPI-5VDIMM&3VSB	
33 PM-SY8288RAC-1.05V/GS7133-2.5V	
34 DDR PWR VPP25/VTM-MP2147	
35 DDR Power-RT8231AGQW	
36 CPU Power 1P8V-MP2147	



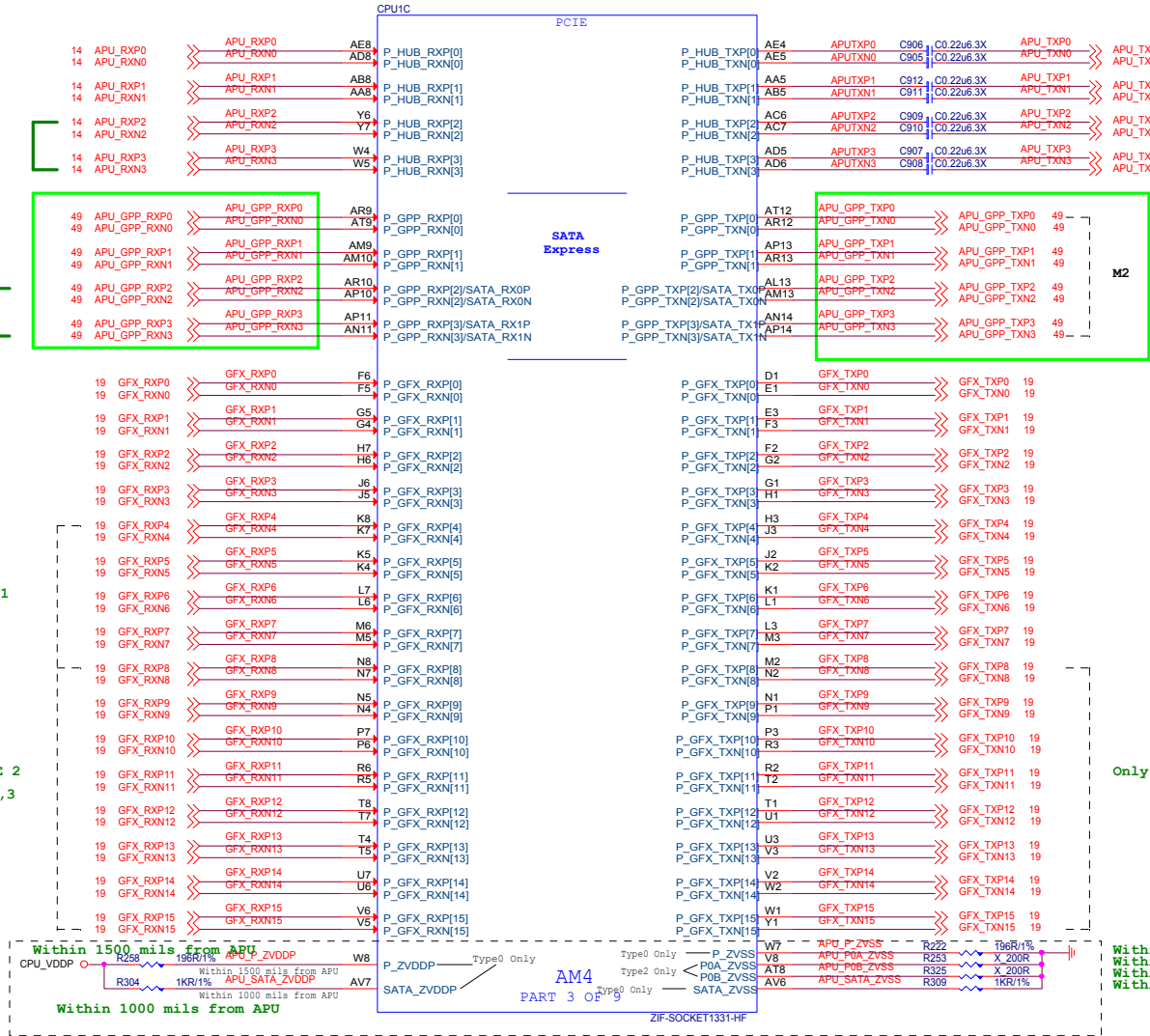
Not supported HUB on TYPE 1

Not supported PCIE on TYPE 0,1

TYPE	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

Not supported GFX 4~15 on TYPE,1

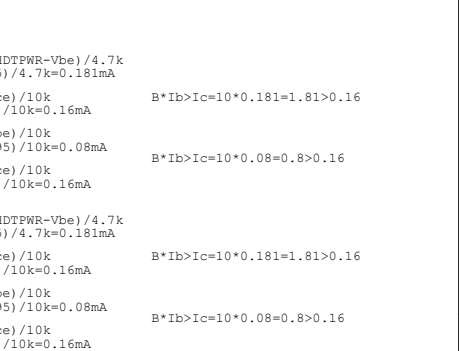
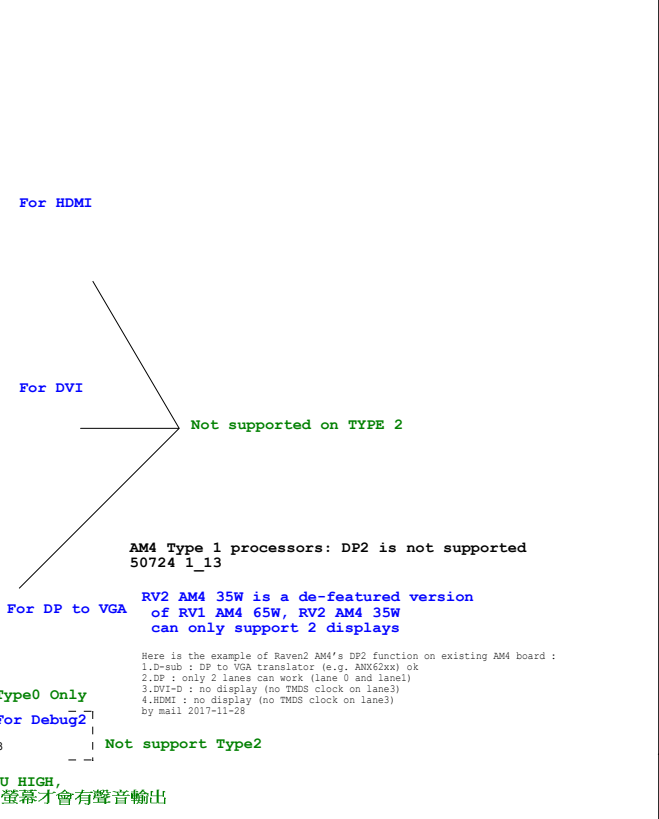
Only supported on TYPE 2  
Not supported GFX 8~15 on TYPE 0,3



Not supported PCIE on TYPE 0,1

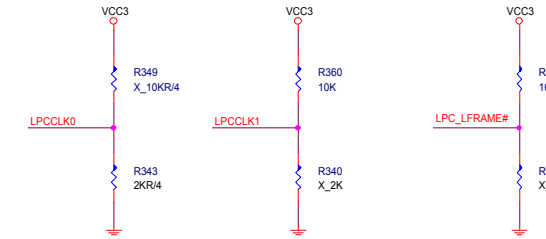
Only supported on TYPE 2

Within 1500 mils from APU  
Within 1500 mils from APU  
Within 1000 mils from APU  
Within 1000 mils from APU

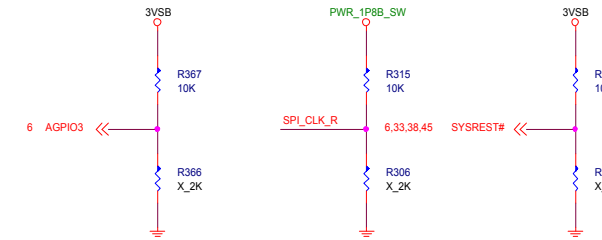




# Strapping Options

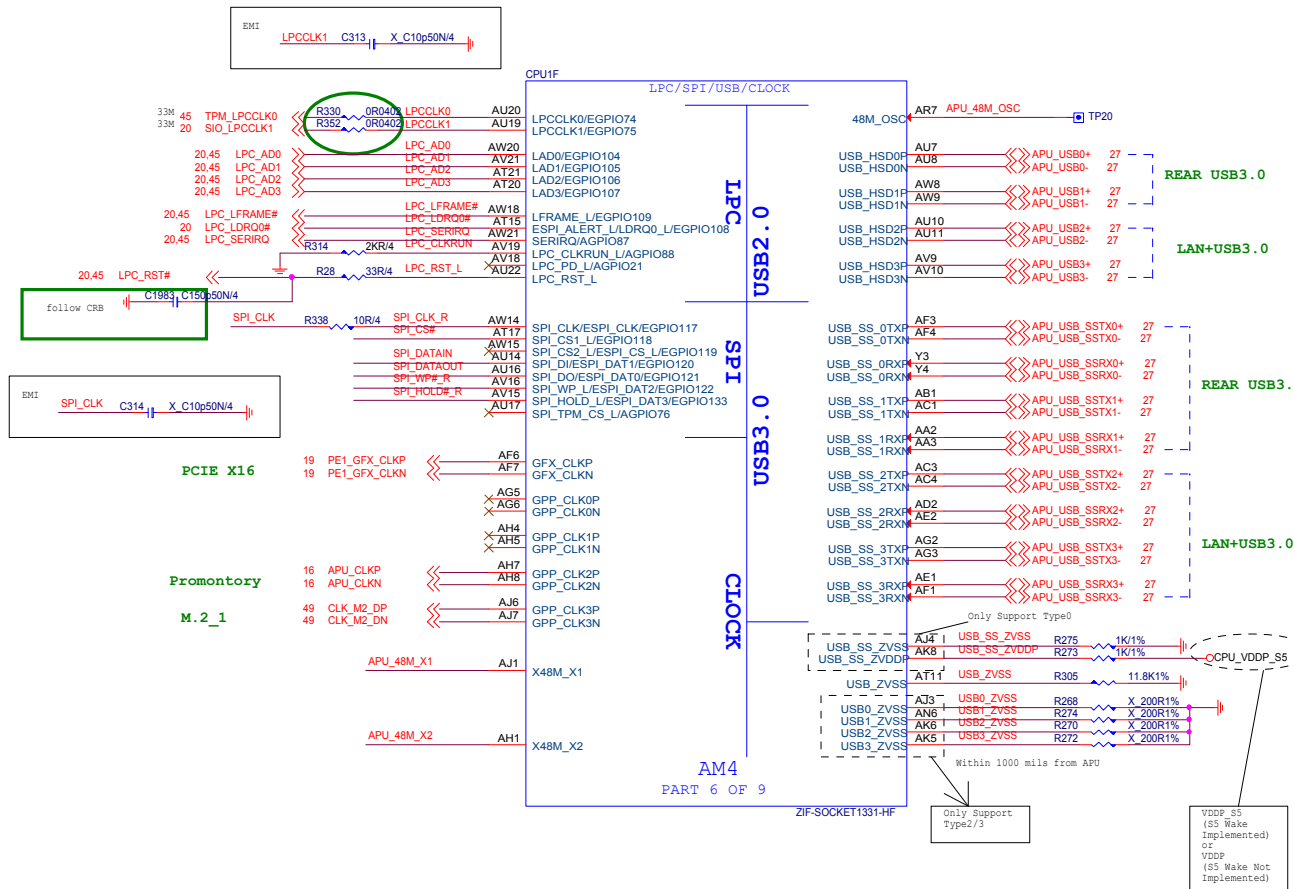


	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ????	LPC ROM (Default)

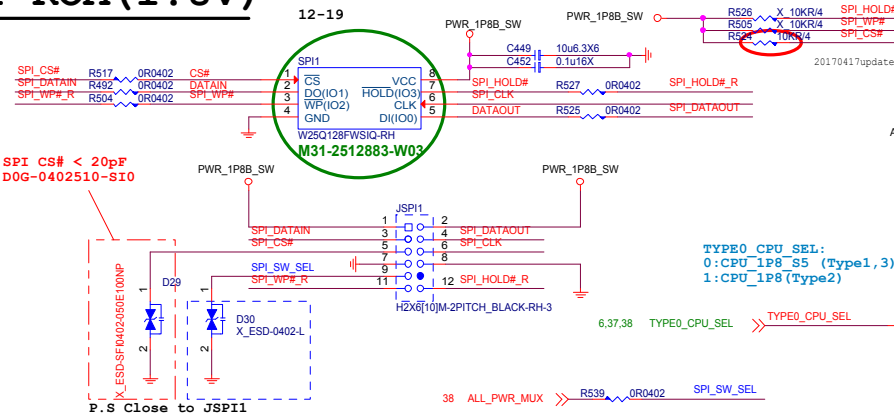


	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

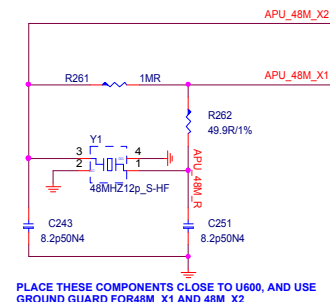
	RTCCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board



## SPI ROM (1.8V)

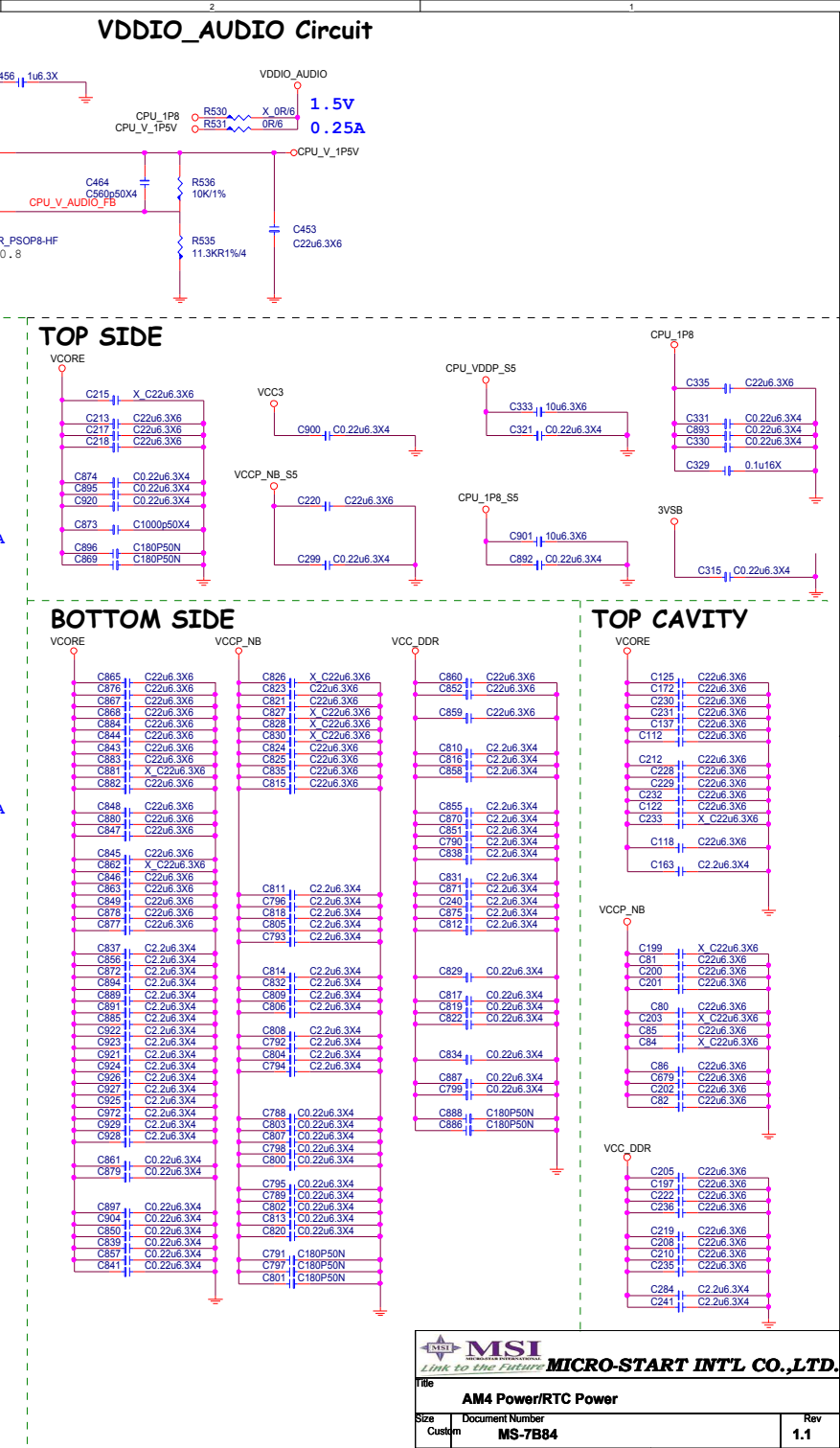
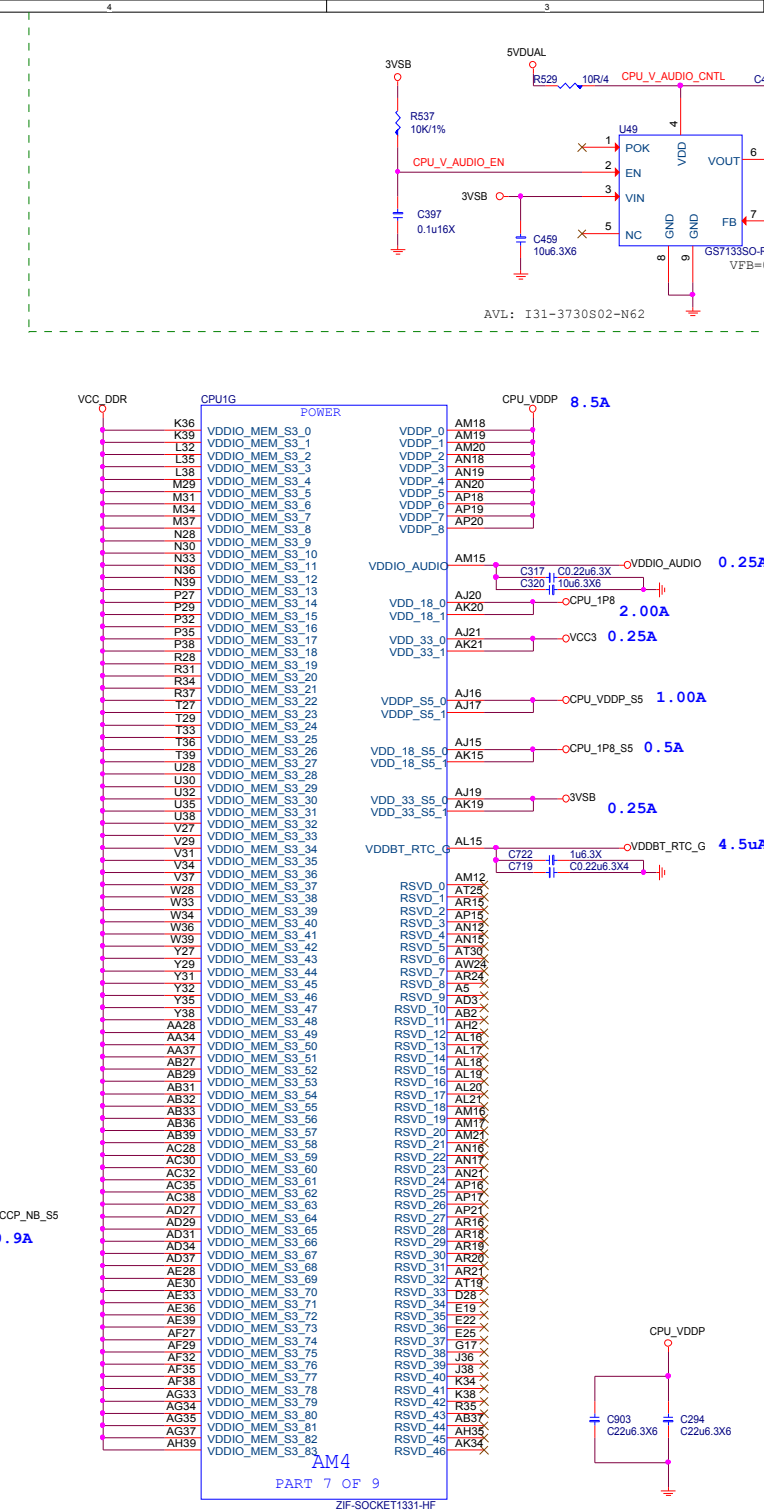


Layout: Place x'tal within 1.5 inch of APU



PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 48M\_X1 AND 48M\_X2



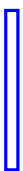




GND

AM4  
PART 9 OF 9

A1



A

A

A

A

A

A

A

A

A

A

A

A

A

A

A

A

A

DIMMA1A

DQS17P

DQS17N

DQS16P

DQS16N

DQS15P

DQS15N

DQS14P

DQS14N

DQS13P

DQS13N

DQS12P

DQS12N

DQS11P

DQS11N

DQS10P

DQS10N

DQS9P

DQS9N

DQS8P

DQS8N

DQS7P

DQS7N

DQS6P

DQS6N

DQS5P

DQS5N

DQS4P

DQS4N

DQS3P

DQS3N

DQS2P

DQS2N

DQS1P

DQS1N

DQS0P

DQS0N

CK1P

CK1N

CK0P

CK0N

C2

S3\_N\_C1

S2\_N\_C0

S1\_N

S0\_N

CKE1

CKE0

ODT1

ODT0

CB-7

CB-6

CB-5

CB-4

CB-3

CB-2

CB-1

CB-0

RESET\_N

EVENT\_N

ALERT\_N

ACT\_N

PAR

SAVE\_N\_NC

RFU-0

RFU-1

RFU-2

DDRIV-288P\_BLACK-RH-21

轉正式Footprint

DQ-63

DQ-62

DQ-61

DQ-60

DQ-59

DQ-58

DQ-57

DQ-56

DQ-55

DQ-54

DQ-53

DQ-52

DQ-51

DQ-50

DQ-49

DQ-48

DQ-47

DQ-46

DQ-45

DQ-44

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DQ-19

DQ-18

DQ-17

DQ-16

DQ-15

DQ-14

DQ-13

DQ-12

DQ-11

DQ-10

DQ-9

DQ-8

DQ-7

DQ-6

DQ-5

DQ-4

DQ-3

DQ-2

DQ-1

DQ-0

BG-1

BG-0

BA-1

BA-0

A17

A16\_RAS\_N

A15\_CAS\_N

A14\_WE\_N

A13

A12

A11

A10

A9

A8

A7

A6

A5

A4

A3

A2

A1

A0

SCL

SDA

SA-2

SA-1

SA-0

DIMM1 (CHANNEL-A) -A0  
ADDRESS = 0:0 [SA1:SA0]

6.39.43.48 SCLK0 SCLK0 R427 OR/4 SMB\_CLK\_DIMM 11  
6.39.43.48 SDATA0 SDATA0 R431 OR/4 SMB\_DATA\_DIMM 11

<< MA\_DATA[63..0] 3

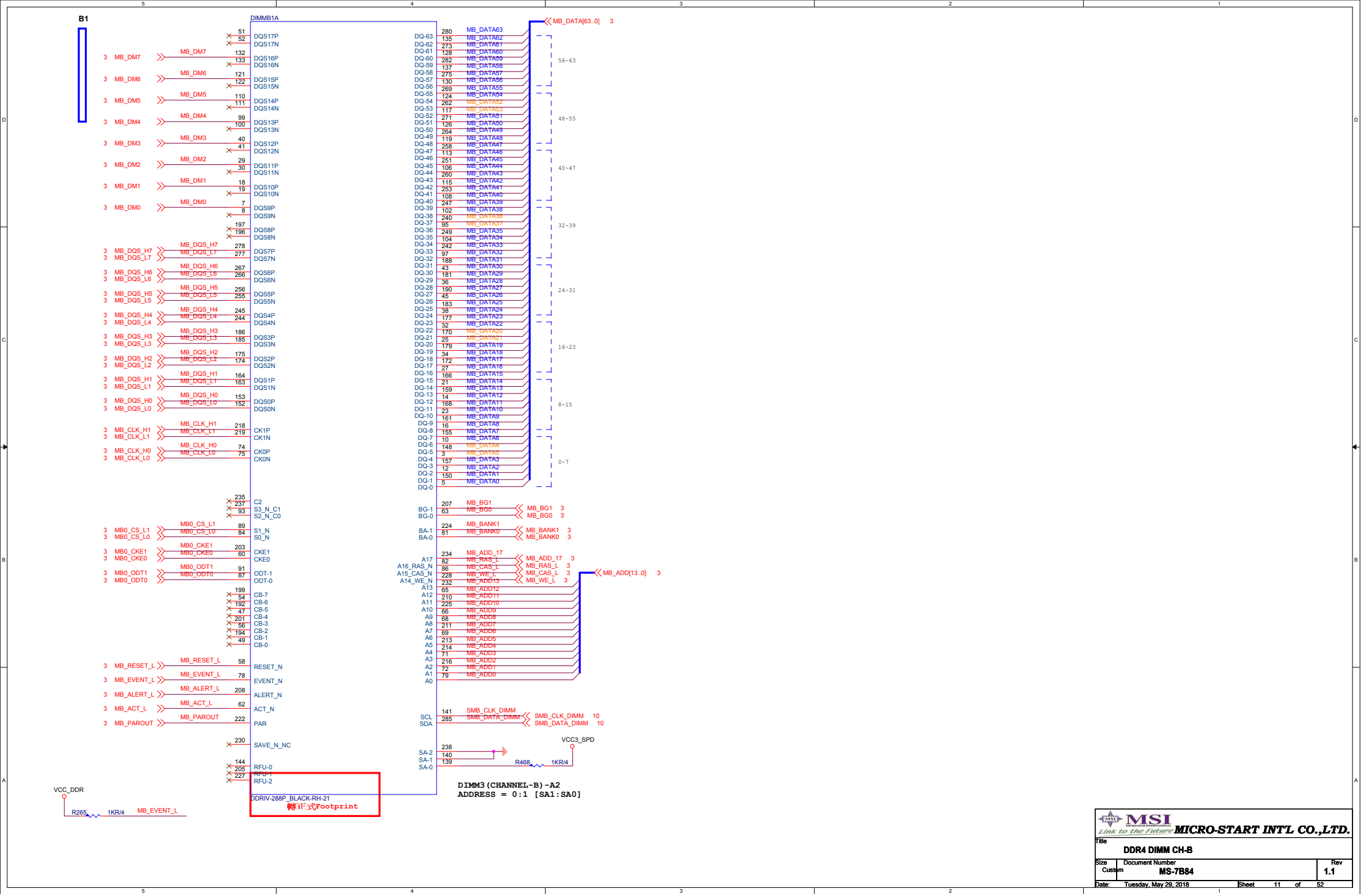
<< MA\_ADD[13..0] 3

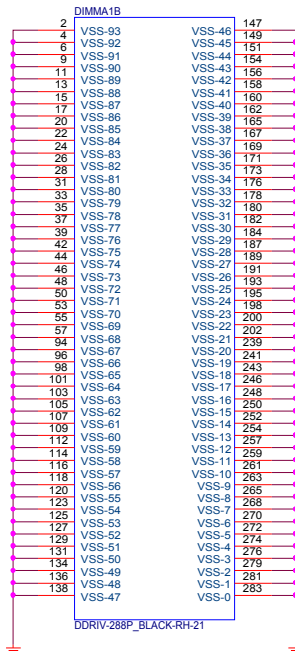
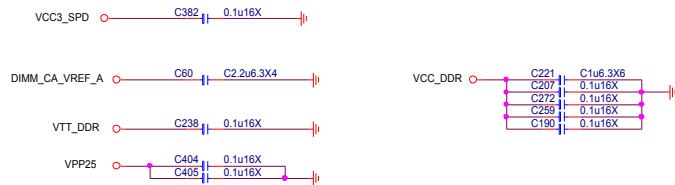
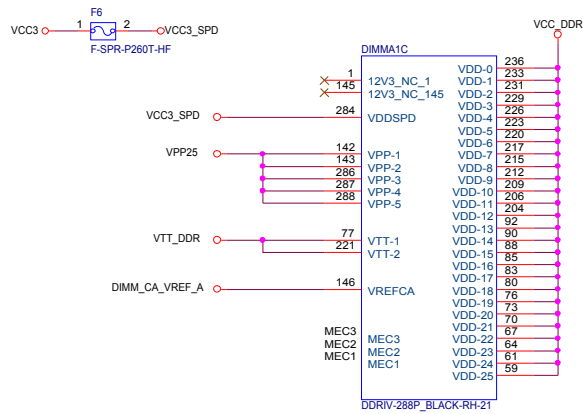
MSI MICRO-START INT'L CO.,LTD.

DDR4 DIMM CH-A

Size Custom Document Number MS-7B84 Rev 1.1

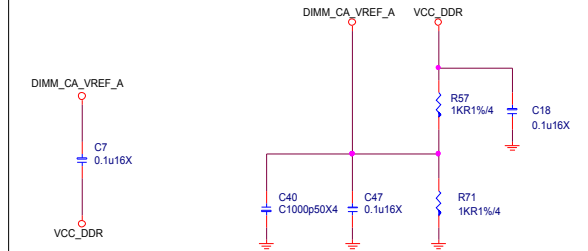
Date: Tuesday, May 29, 2018 Sheet 10 of 52

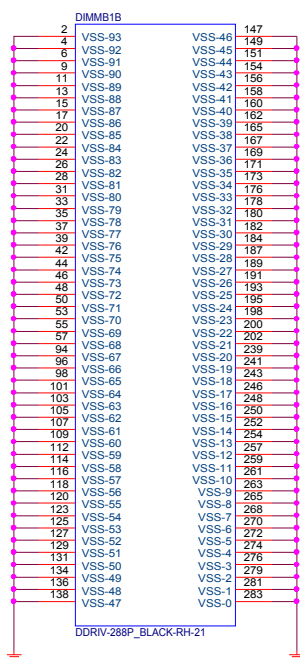
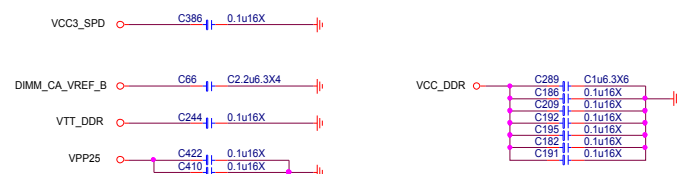
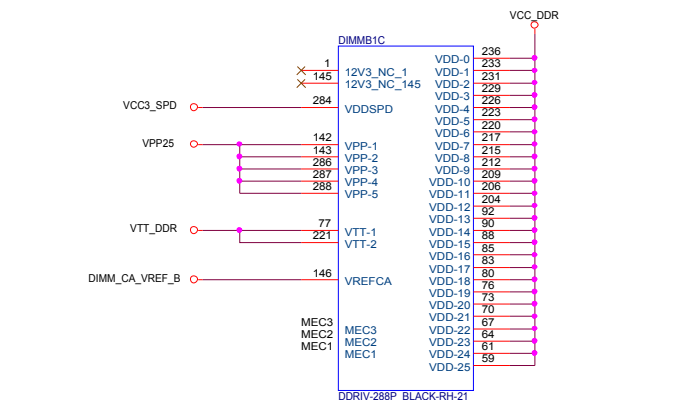




## DDR VREF

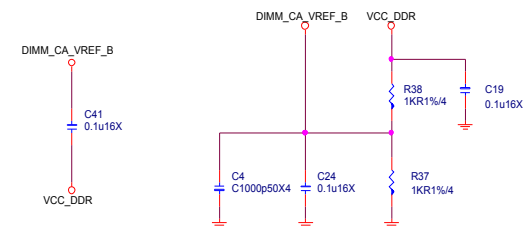
(place resistors close to DIMMs)

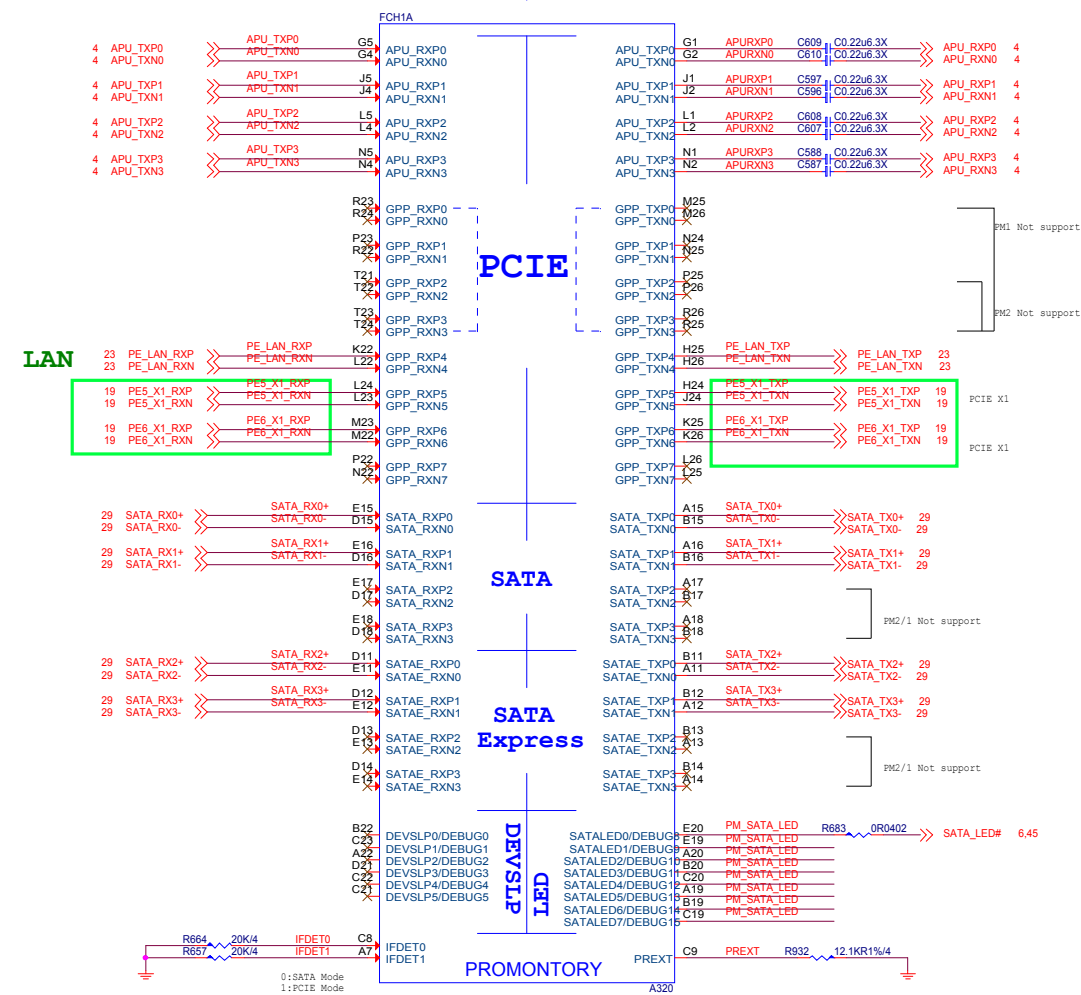




## DDR VREF

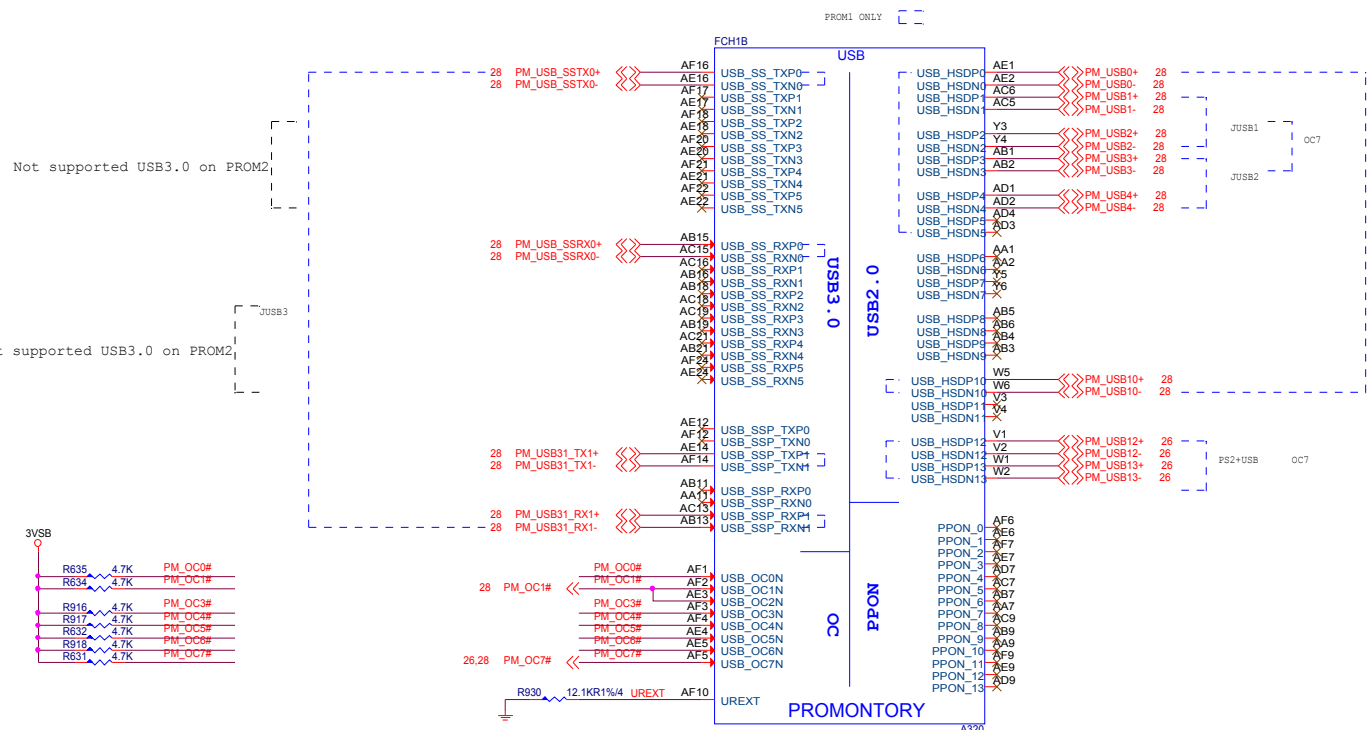
(place resistors close to DIMMs)





SATA Express port0 (IFDET0)  
SATA Express port1 (IFDET1)  
0:SATA Mode  
1:PCIE Mode





## Appendix D USB Port to OC Pin Mapping

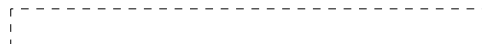
USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

## Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用  
CLK1-3不能用

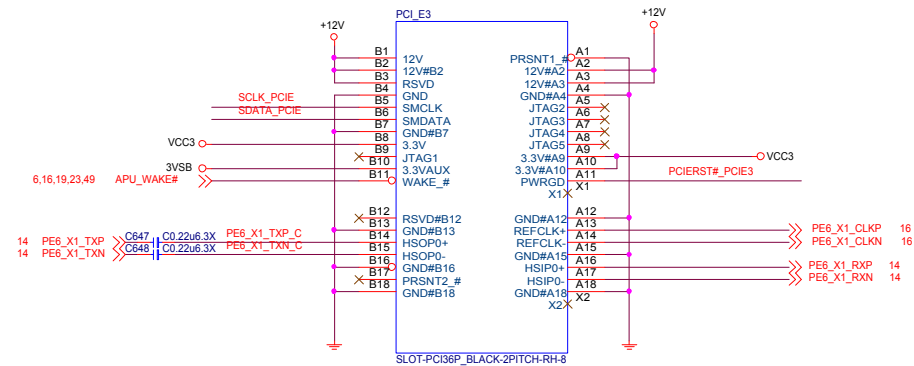
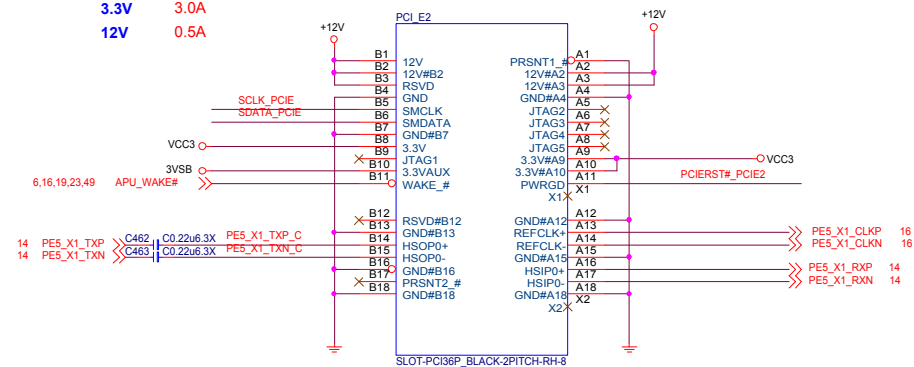
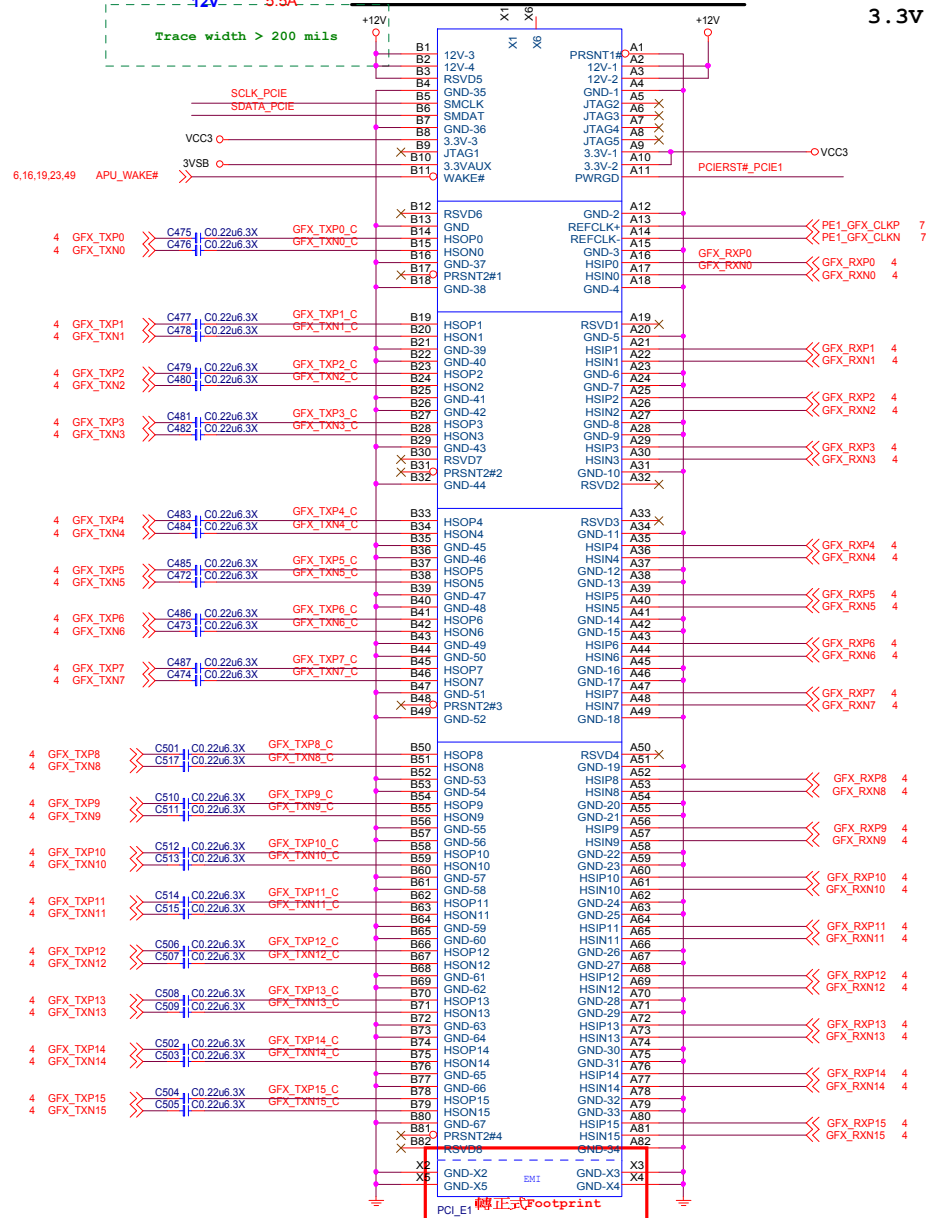


GND

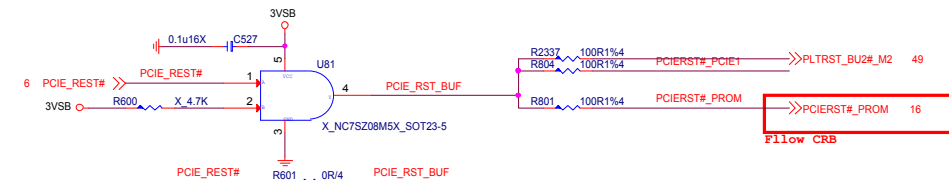
PROMONTORY

PCIEX1 12V 0.5A  
3.3V weak 375mA

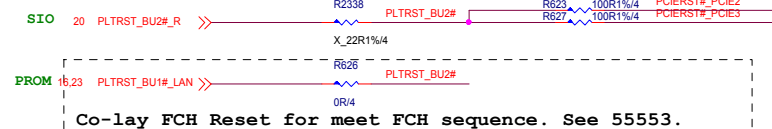
3.3V	3.0A
12V	0.5A



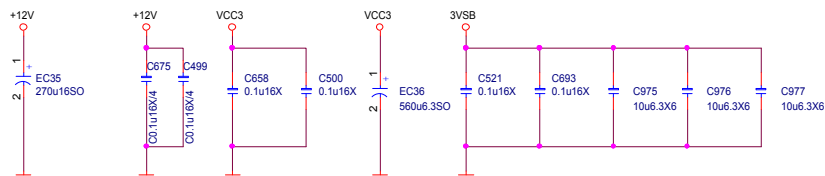
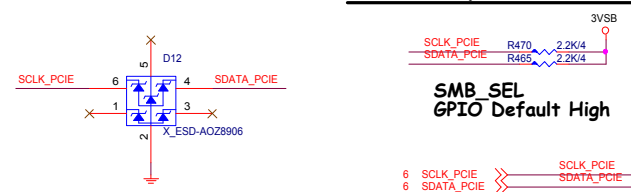
within 500mil



## PROM RESET



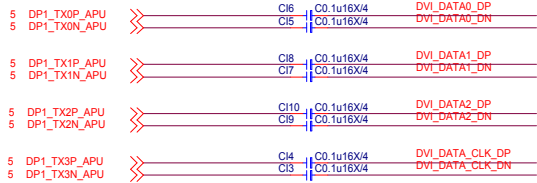
### SMBus separate circuit



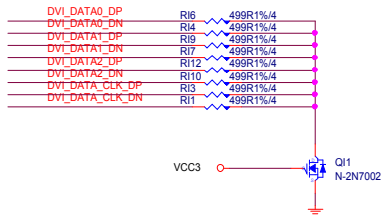
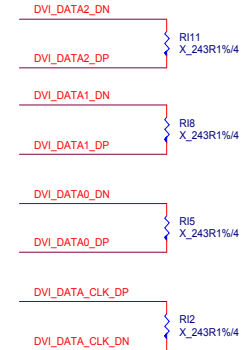




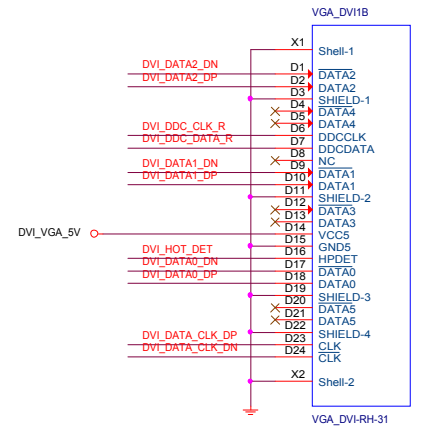
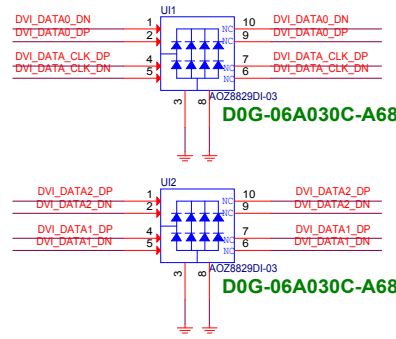
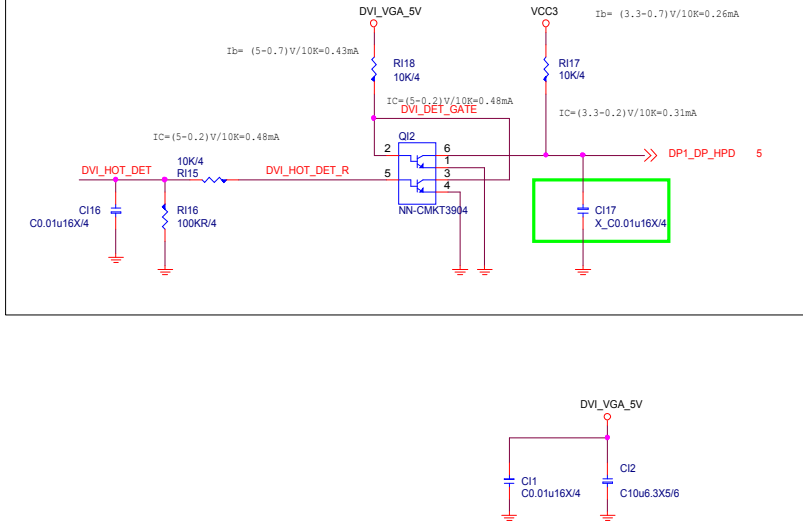
# DVI CONNECTOR



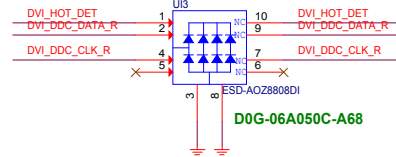
## For EMI



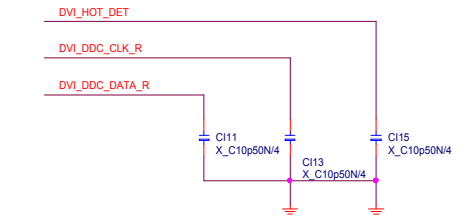
## HPD



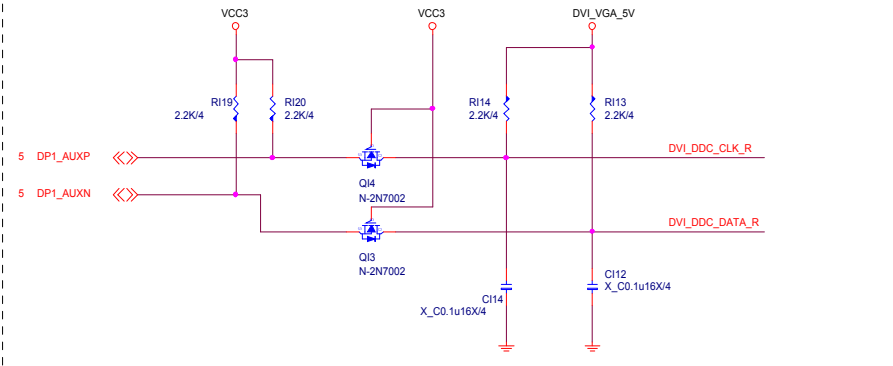
## 注意:耐壓5V零



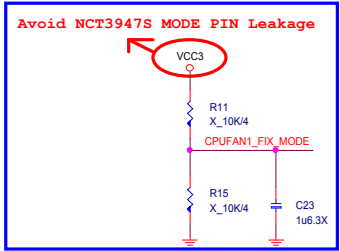
## For EMI



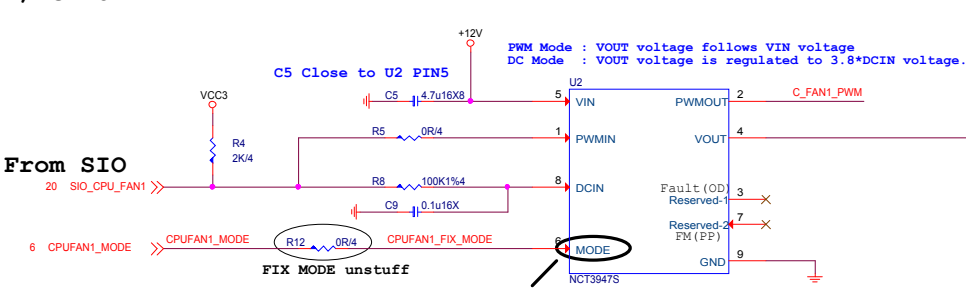
## LEVEL SHIFT using I2C Repeater



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE  
2.GPIO可以由BIOS切换 PWM/DC MODE



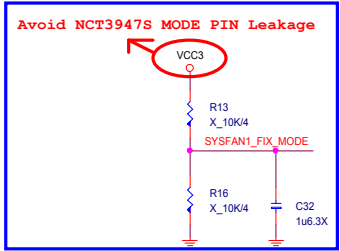
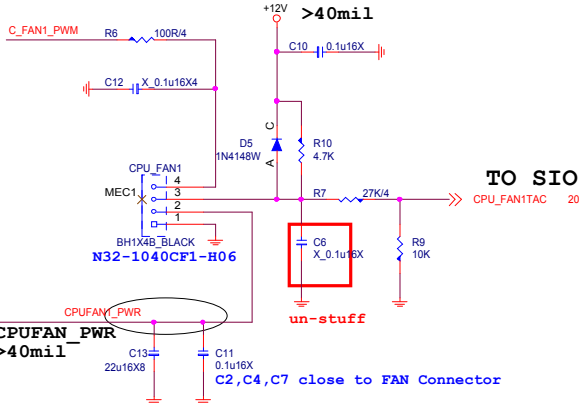
Resever For FIX DC or PWM MODE USE By PM SPEC



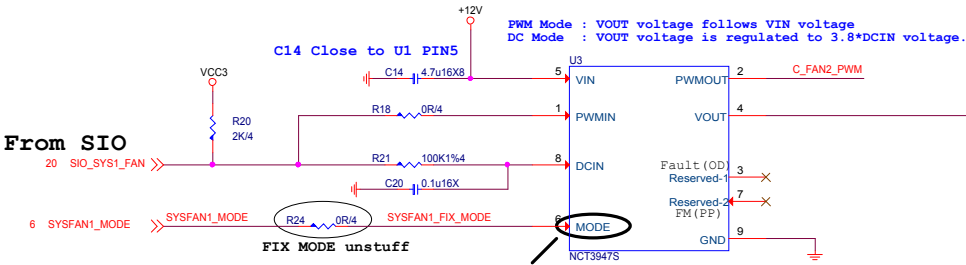
GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default Internall pull up 1.65V



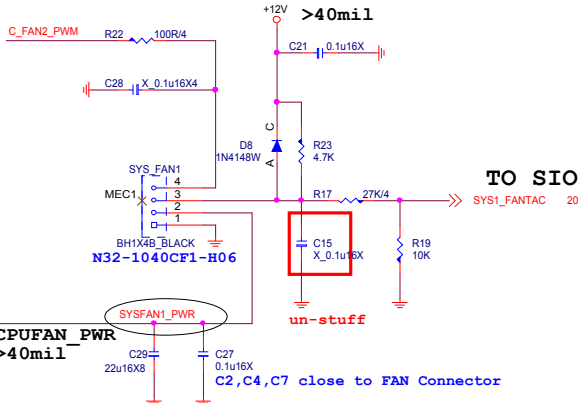
Resever For FIX DC or PWM MODE USE By PM SPEC



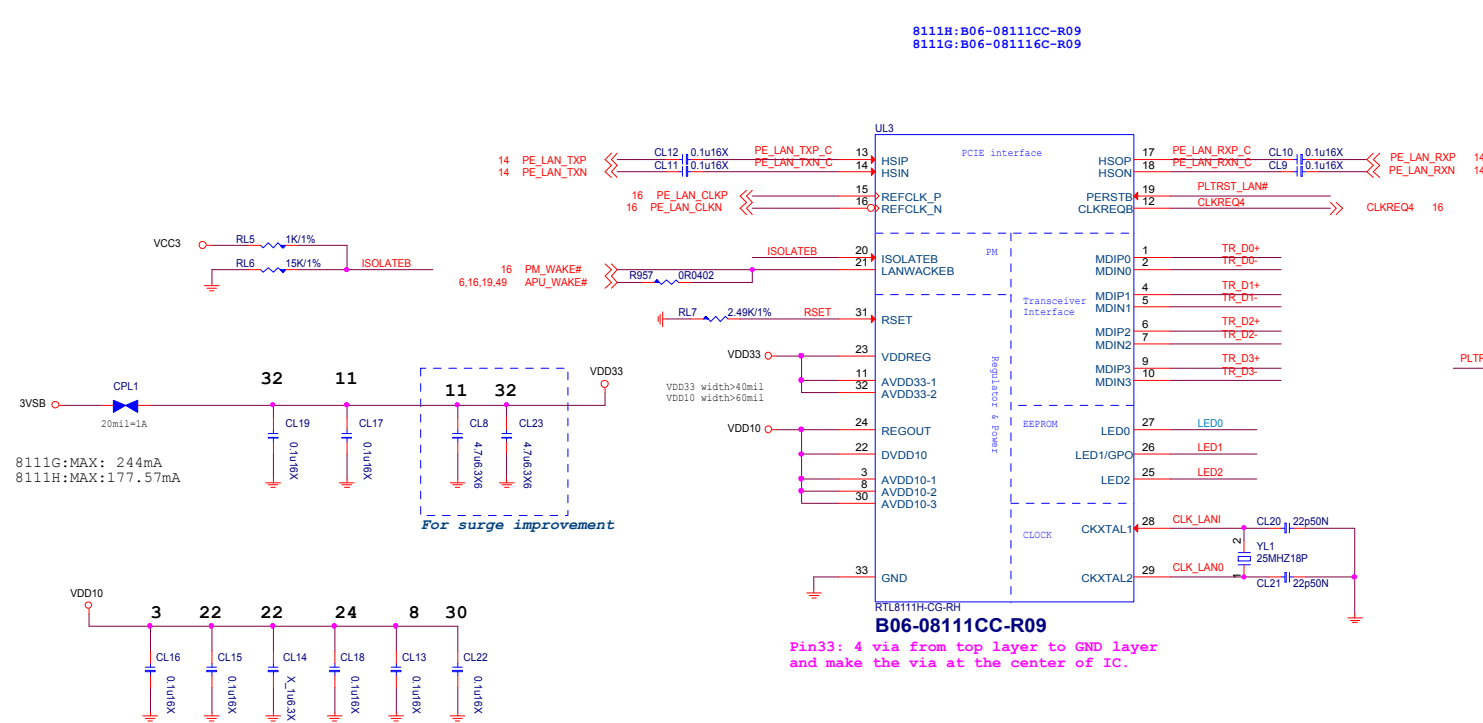
GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default Internall pull up 1.65V



RTL8111G/RTL8111H Giga LAN

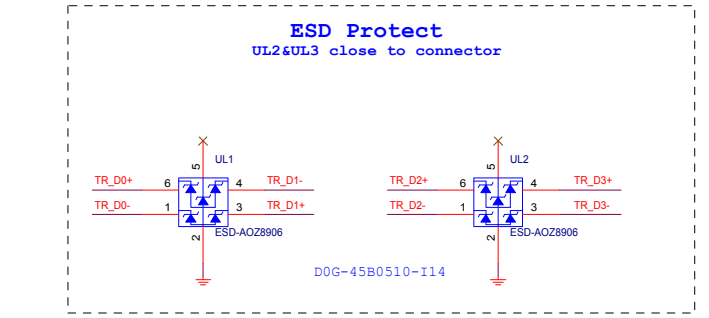
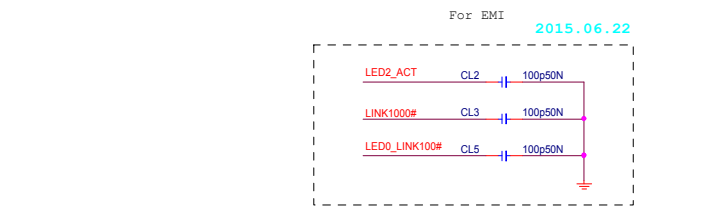
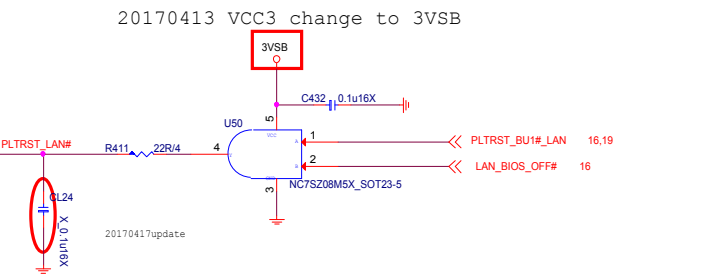
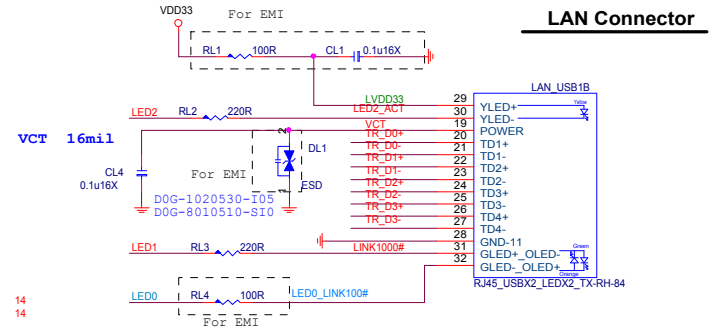


8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



MSI MICRO-START INTL CO.,LTD.

LAN-RTL8111H

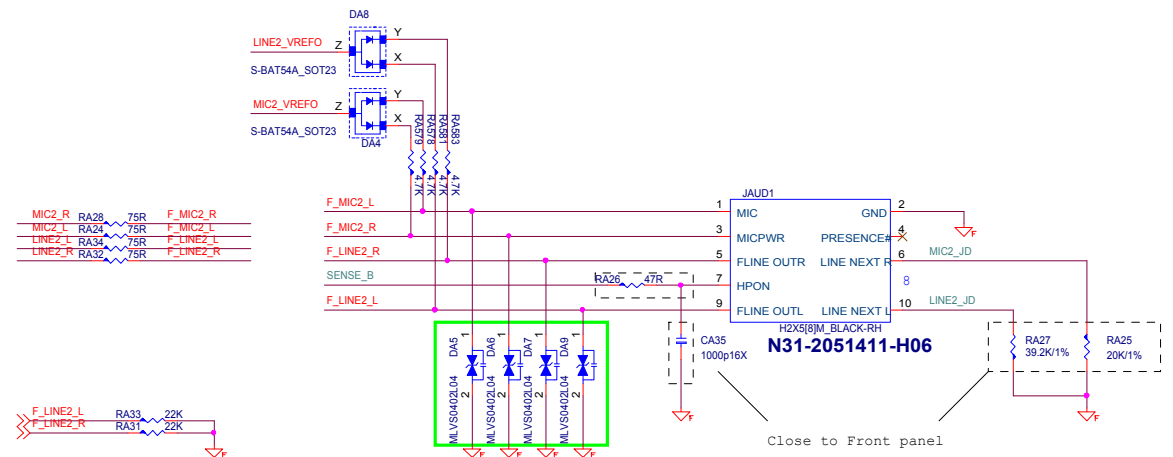
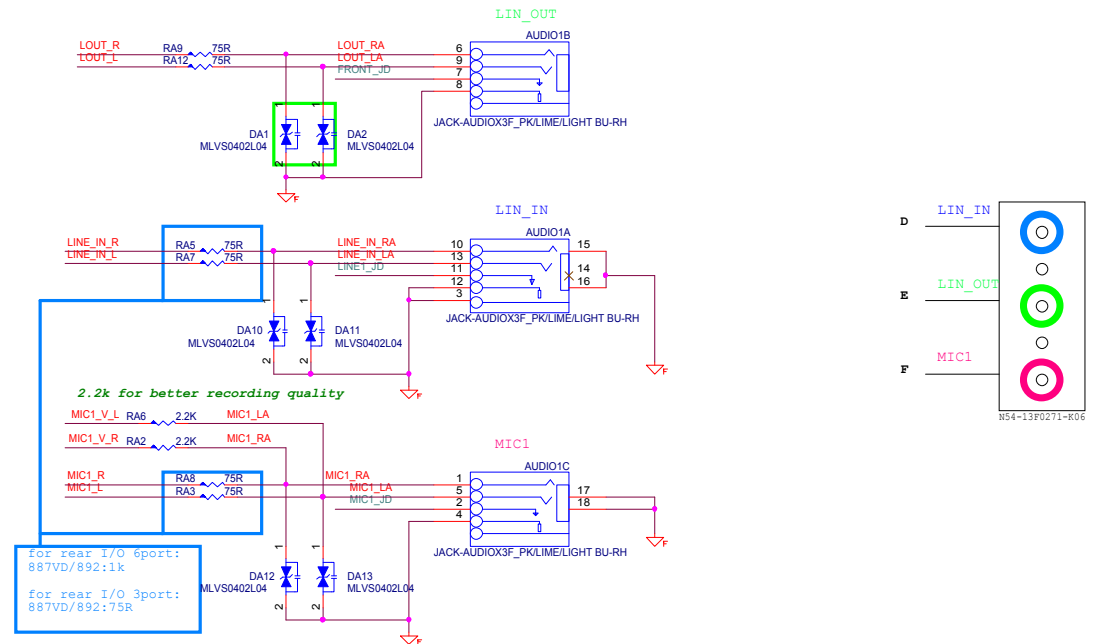
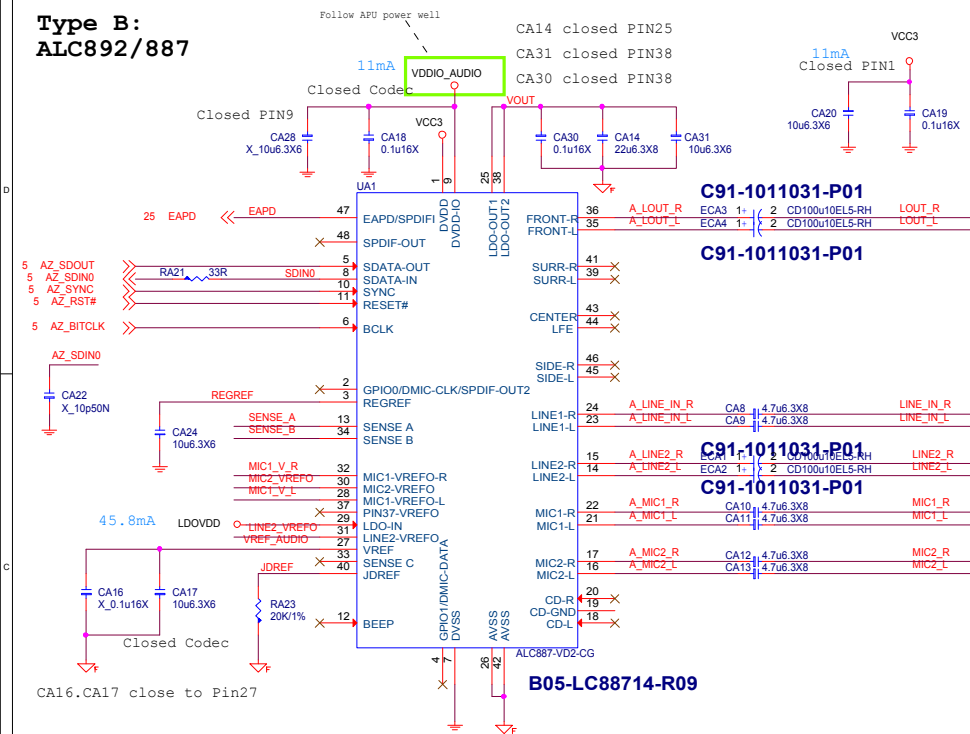
Document Number MS-7B84

Date: Tuesday, May 29, 2018

Sheet 23 of 52

Rev 1.1

Type B:  
ALC892/887



Varister --> cap for cost down

D0G-2710510-I05  
D0G-2950500-SI0

Close to Jack

Close to Front panel  
For HDA/AC97 front cable.

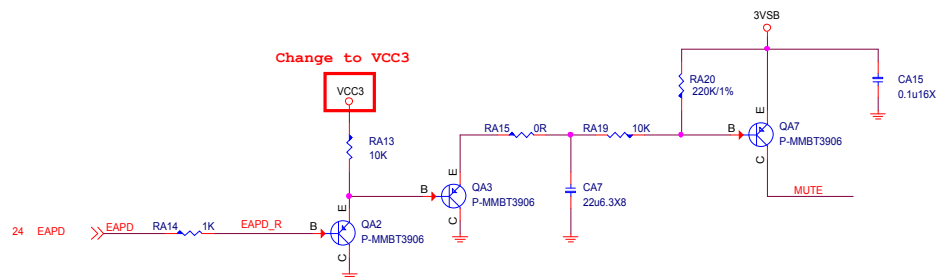


Title	<b>Audio ALC887-1</b>
-------	-----------------------

Size	Document Number	Rev
Custom	<b>MS-7B84</b>	<b>1.1</b>

# Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

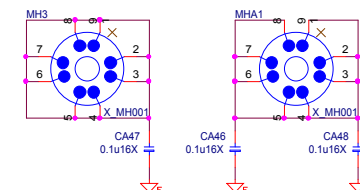


Digital

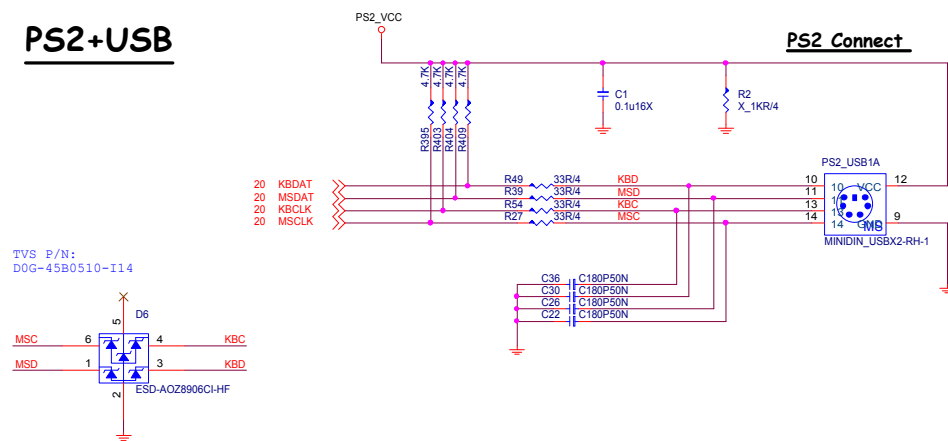
Analog



使用測光LED



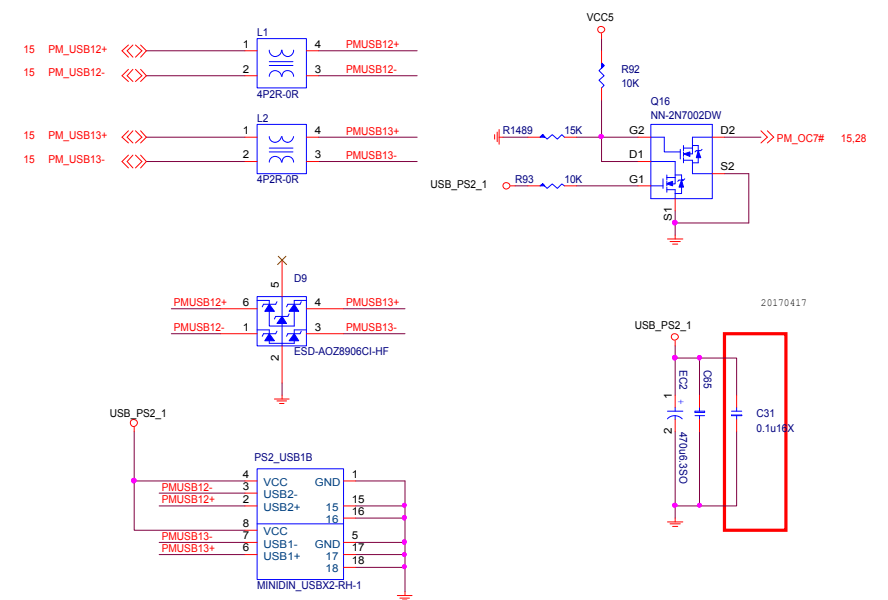
**PS2+USB**



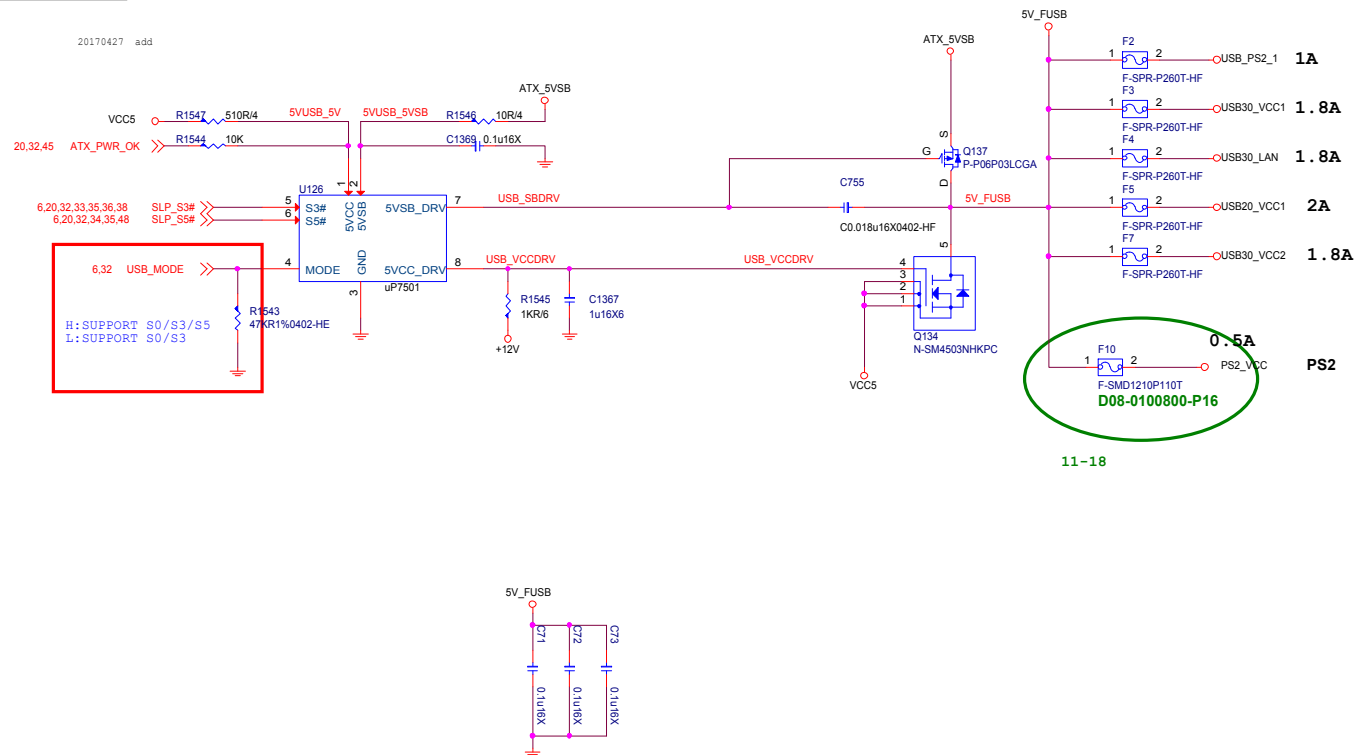
```

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

```

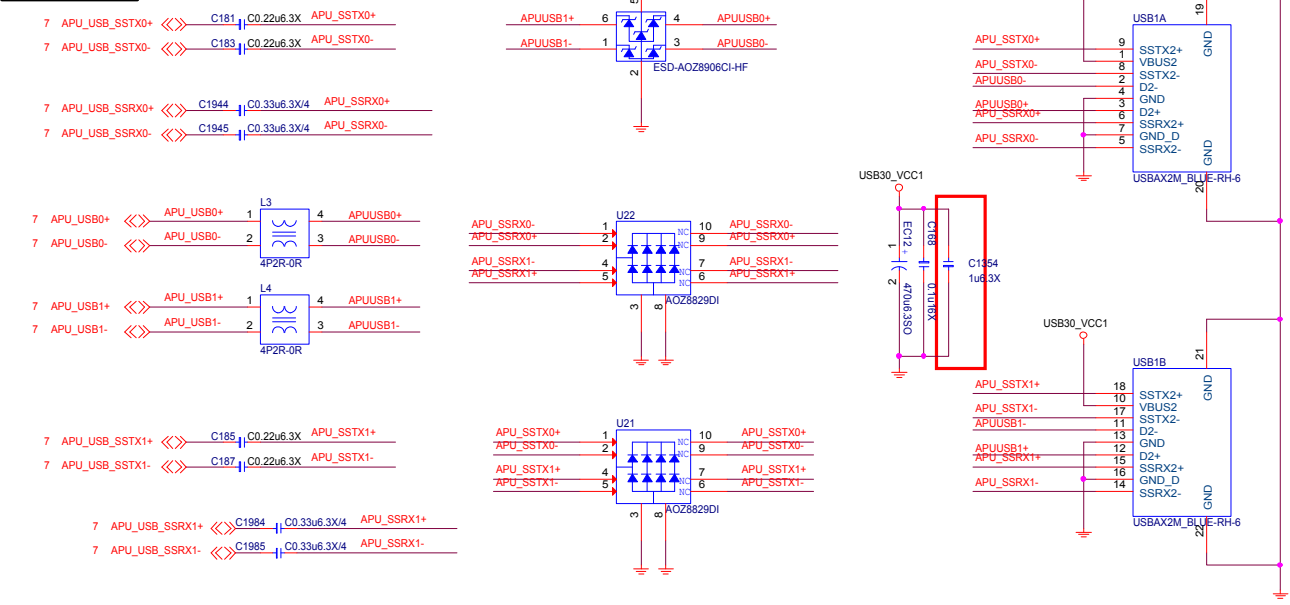


## USB Power

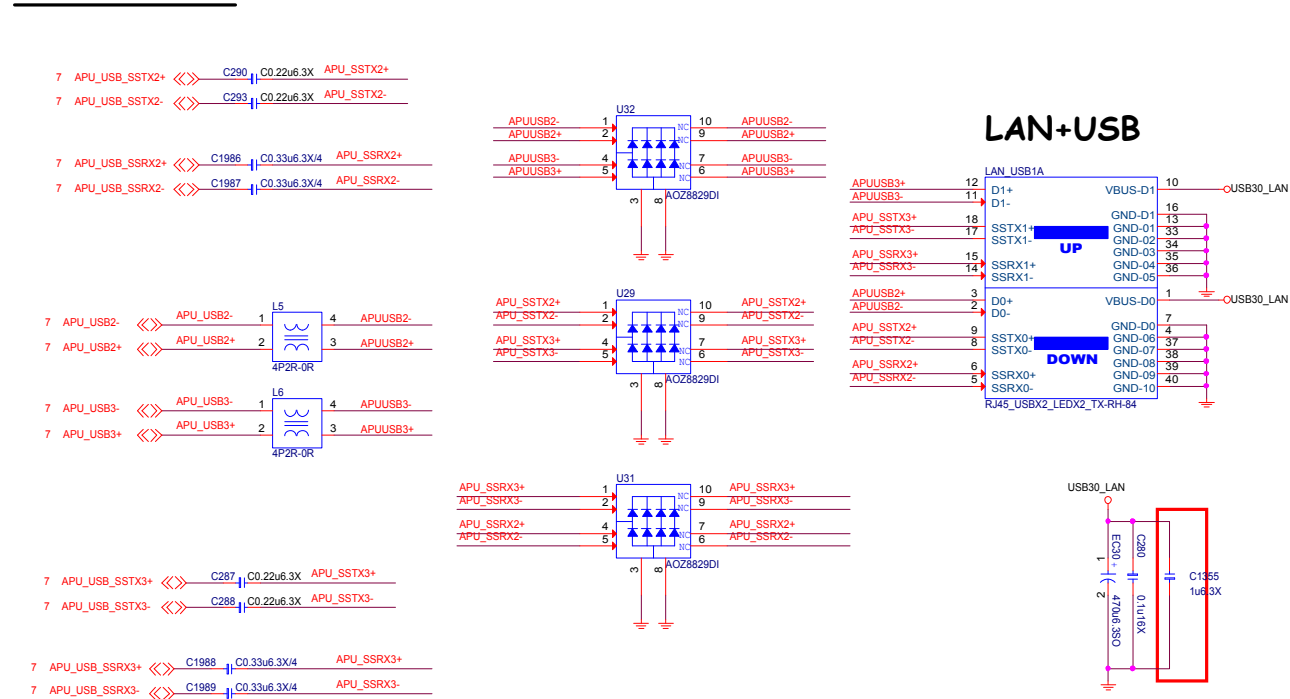




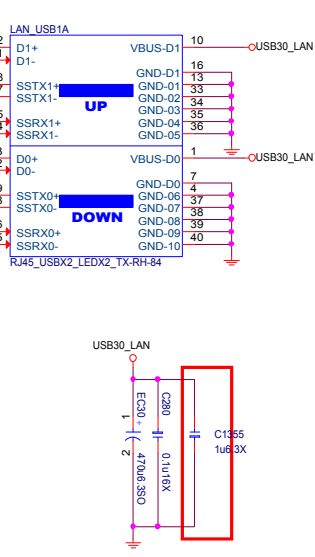
USB 3.0



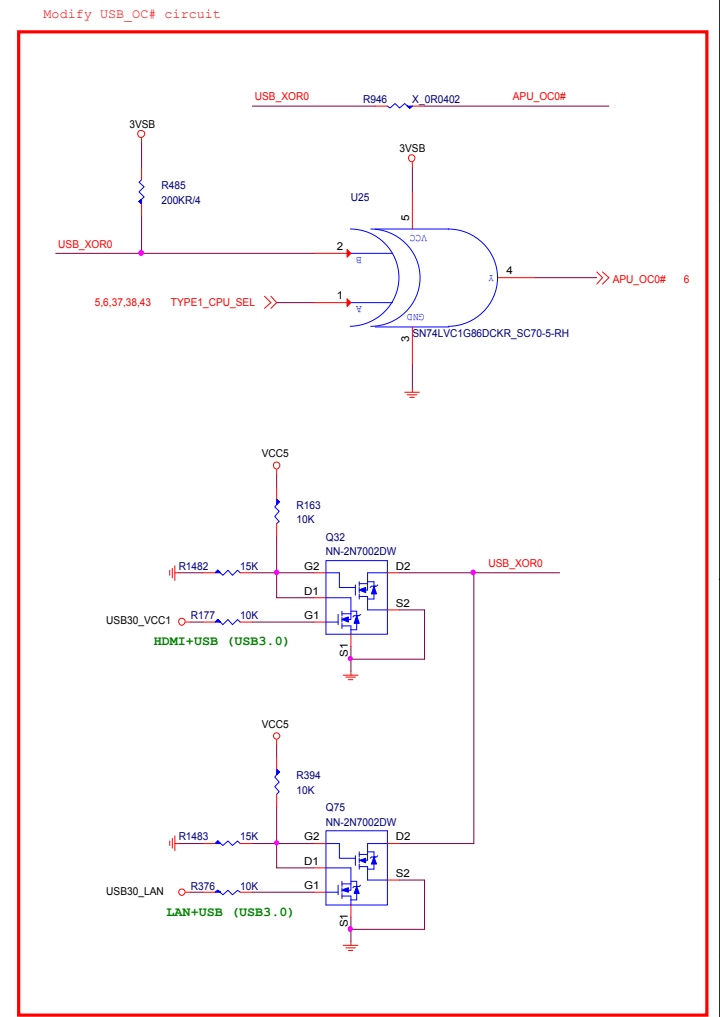
USB3.1 GEN1



LAN+USB



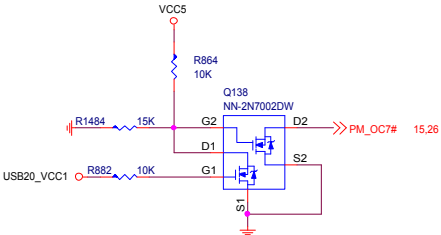
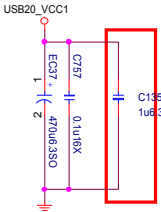
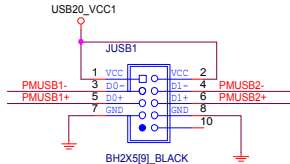
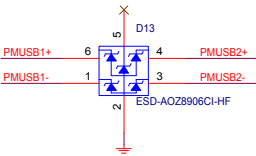
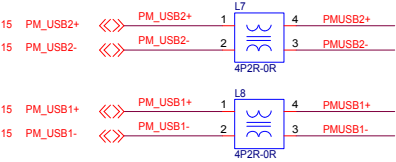
APU\_USB\_OC



	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

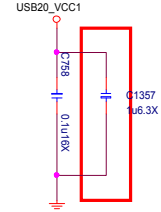
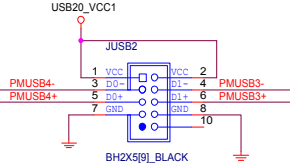
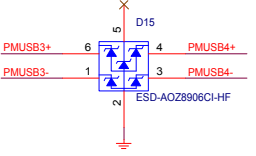
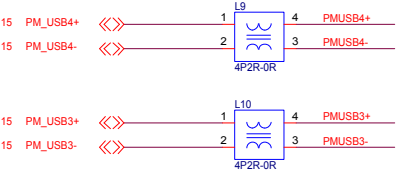
Front USB2.0 (JUSB1)

5V@1A

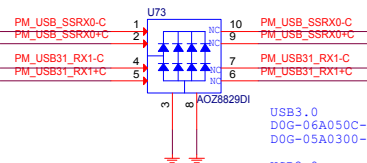
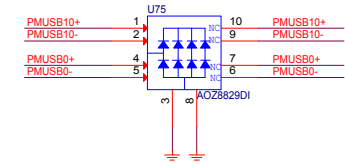
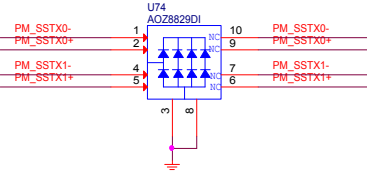
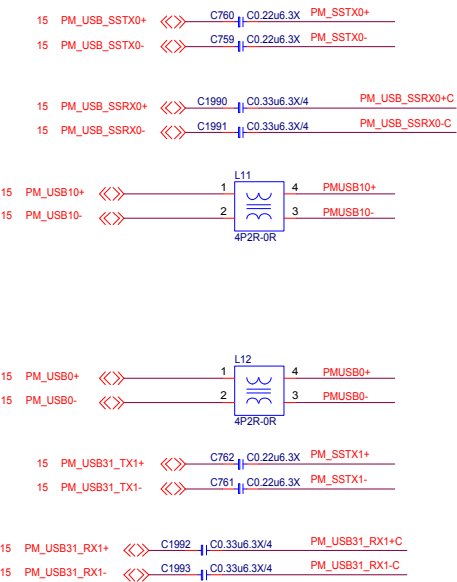


Front USB2.0 (JUSB2)

5V@1A

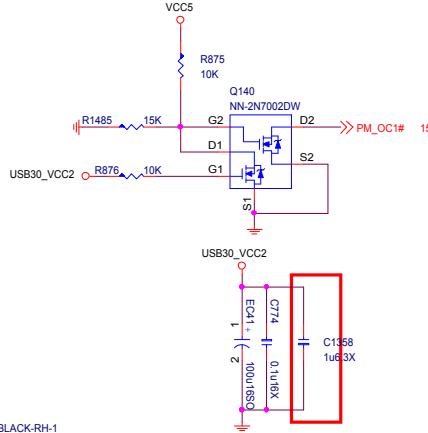
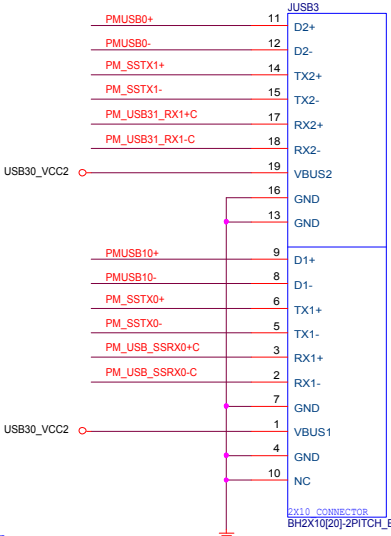


Front USB3.1 GEN1

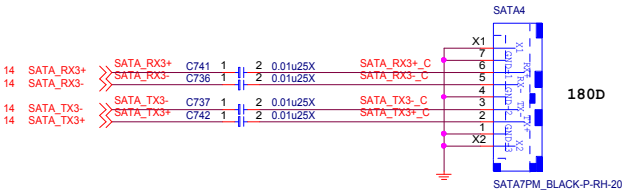
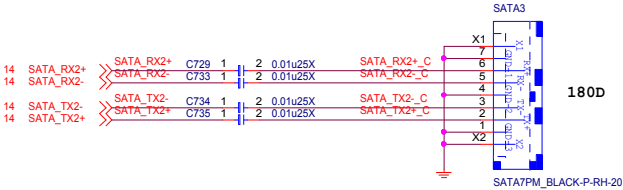
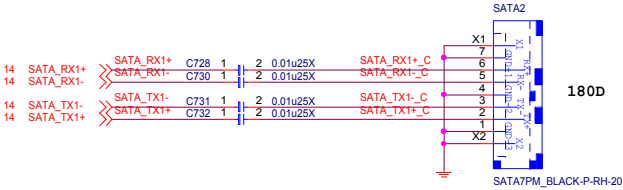
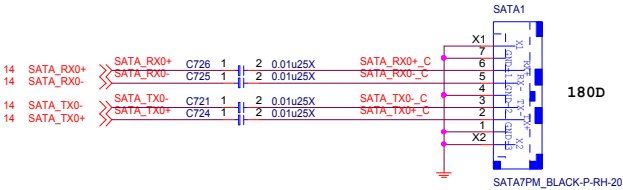


USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL

USB2.0  
D0G-0200529-A68 Main  
D0G-0100619-I05 AVL

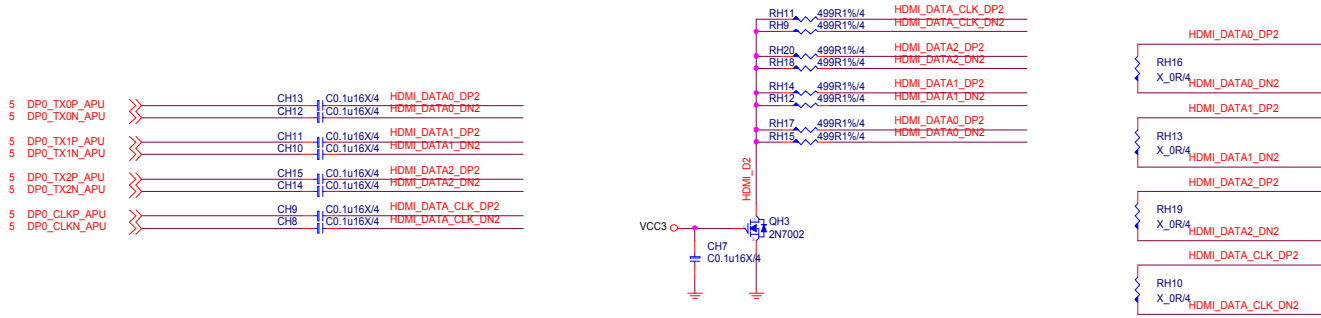


SATA Connector

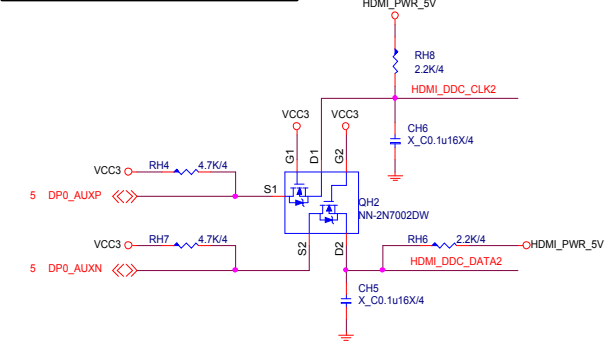


# HDMI CONNECTOR

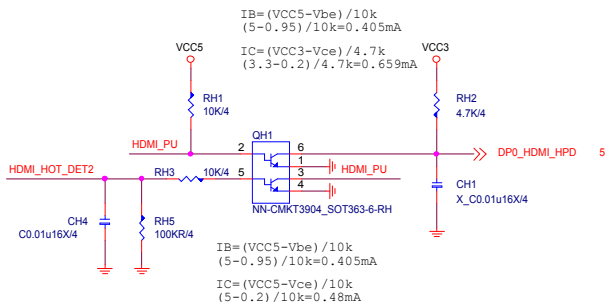
For HDMI 1.4



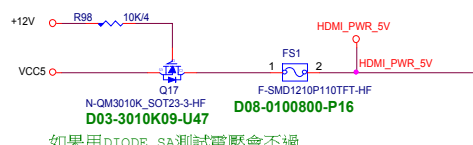
# AUX Level Shifter



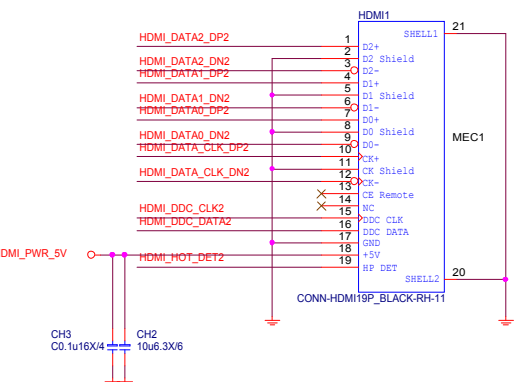
# HPD Circuit



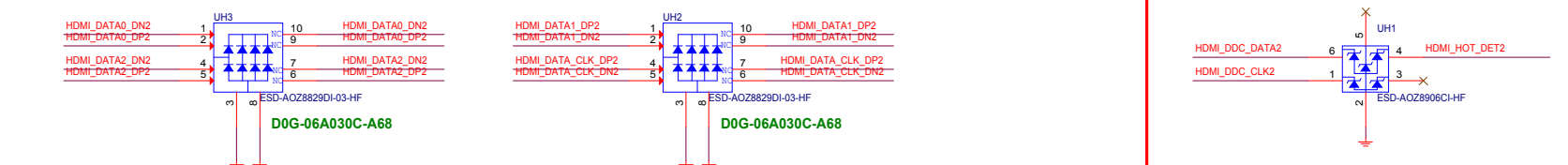
# Connector Power



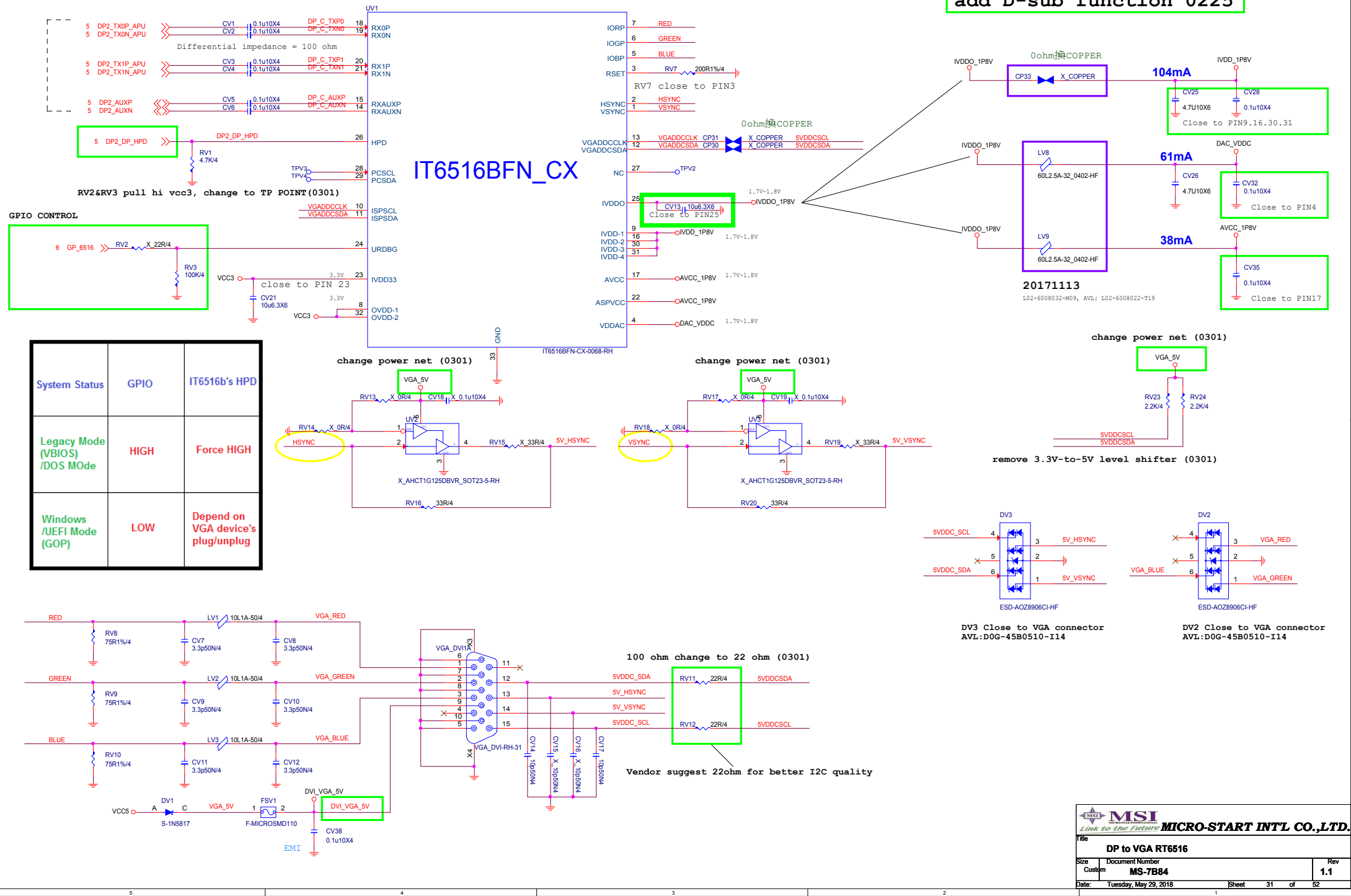
# Connector



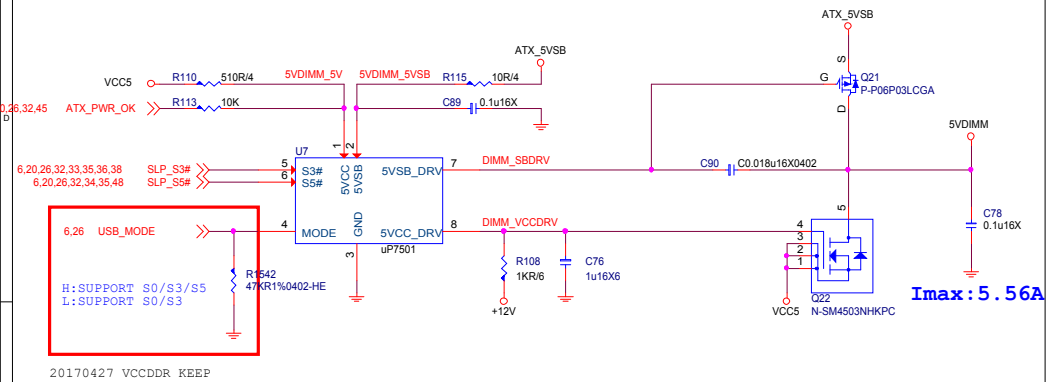
# For EMI



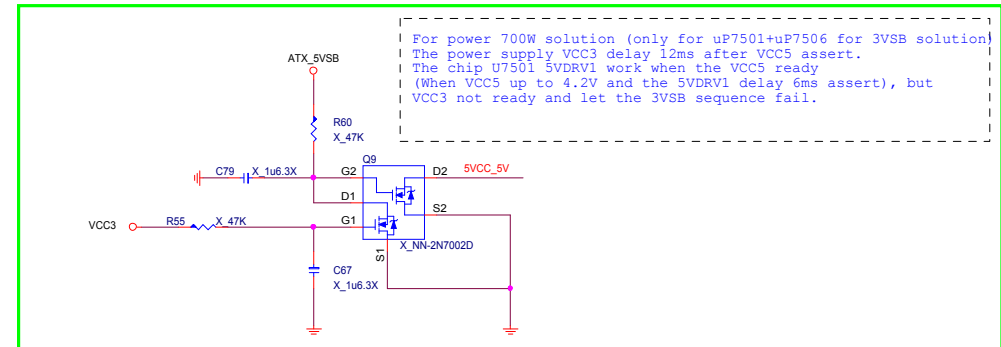
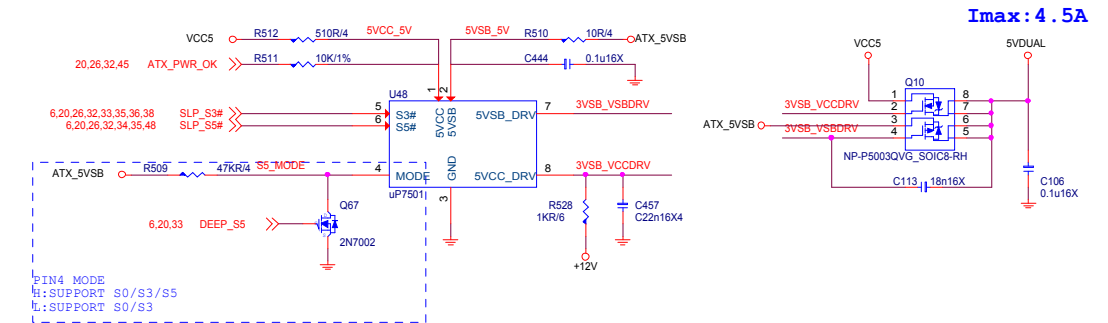
**Note:**  
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



## 5VDIMM FOR DDR

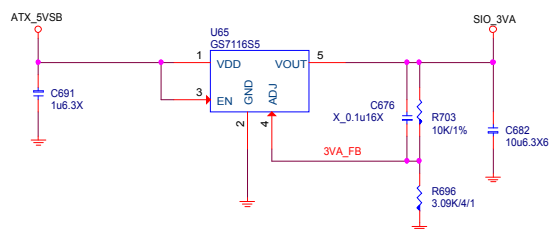


## 5VDUAL For 3VSB、CPU 1.8V、VDDP

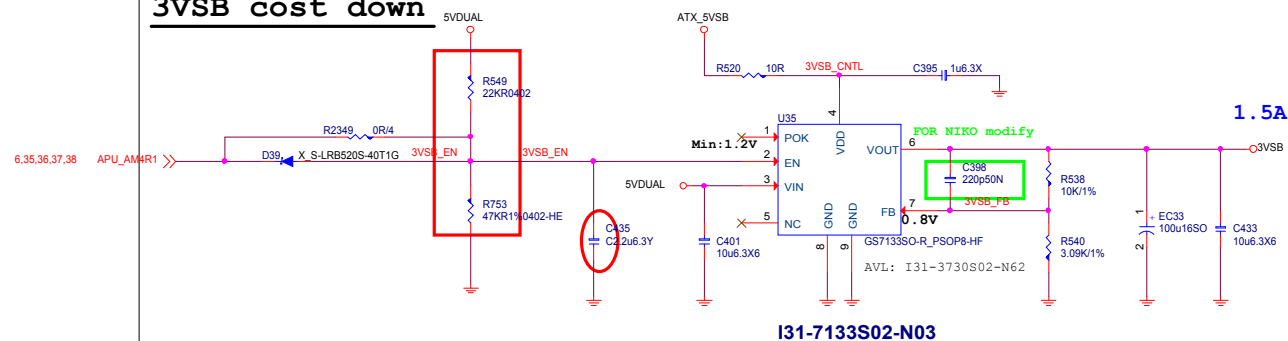


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.

## SIO\_3VA



## 3VSB cost down

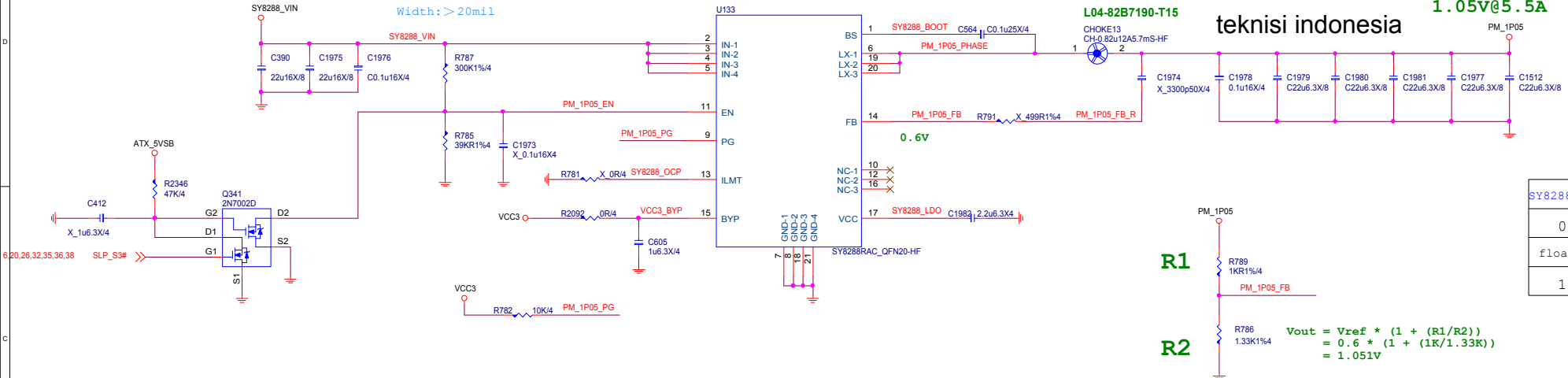




## FOR Promontory 1.05V\_S0

1.05V  
S0:5.5A  
S5:0.05A

+12V L02-3008043-M26  
L20 30L5A  
L48 30L5A  
Input Current= (5.5A\*1.05V)/12V/0.8=0.6A

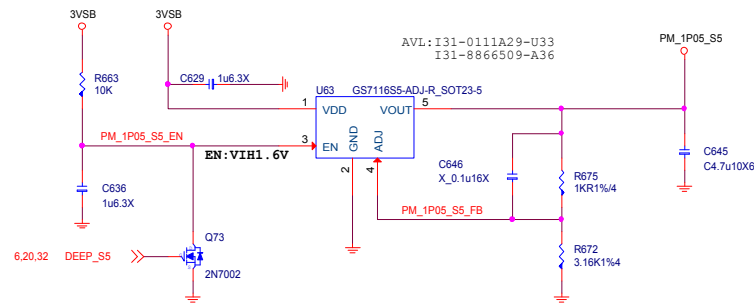


SY8288_OCP	OCP
0	8A
floating	12A
1	16A

$$V_{out} = V_{ref} * (1 + (R1/R2)) = 0.6 * (1 + (1K/1.33K)) = 1.051V$$

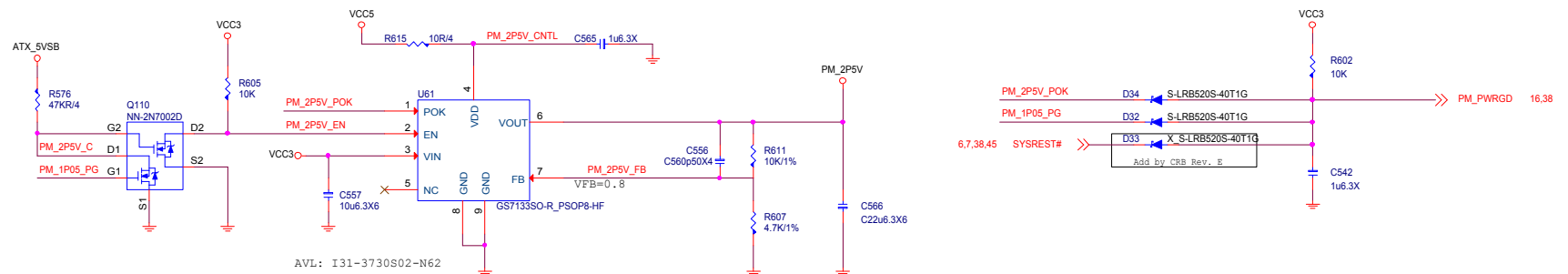
## FOR Promontory 1.05V\_S5

0.05A

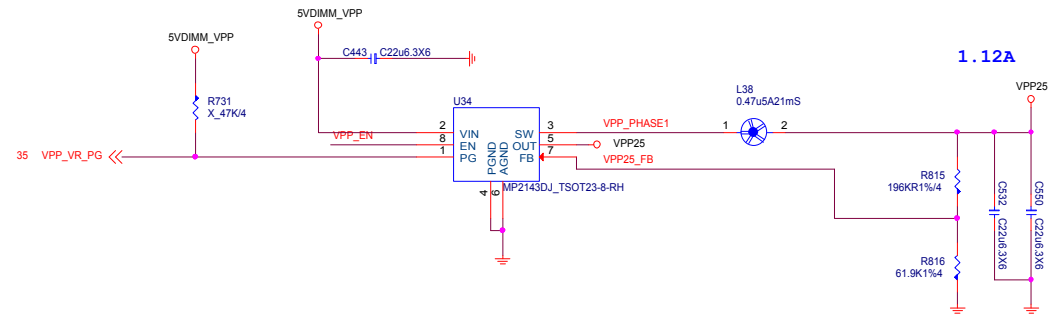
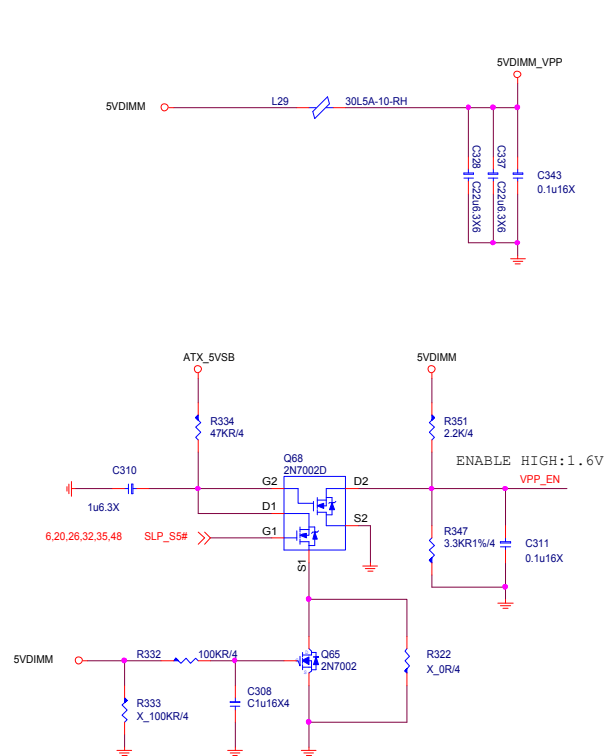


## Promontory-2.5V

2.5V; 900mA



**2DIMM :1.12A FOR DDR VPP2.5V**

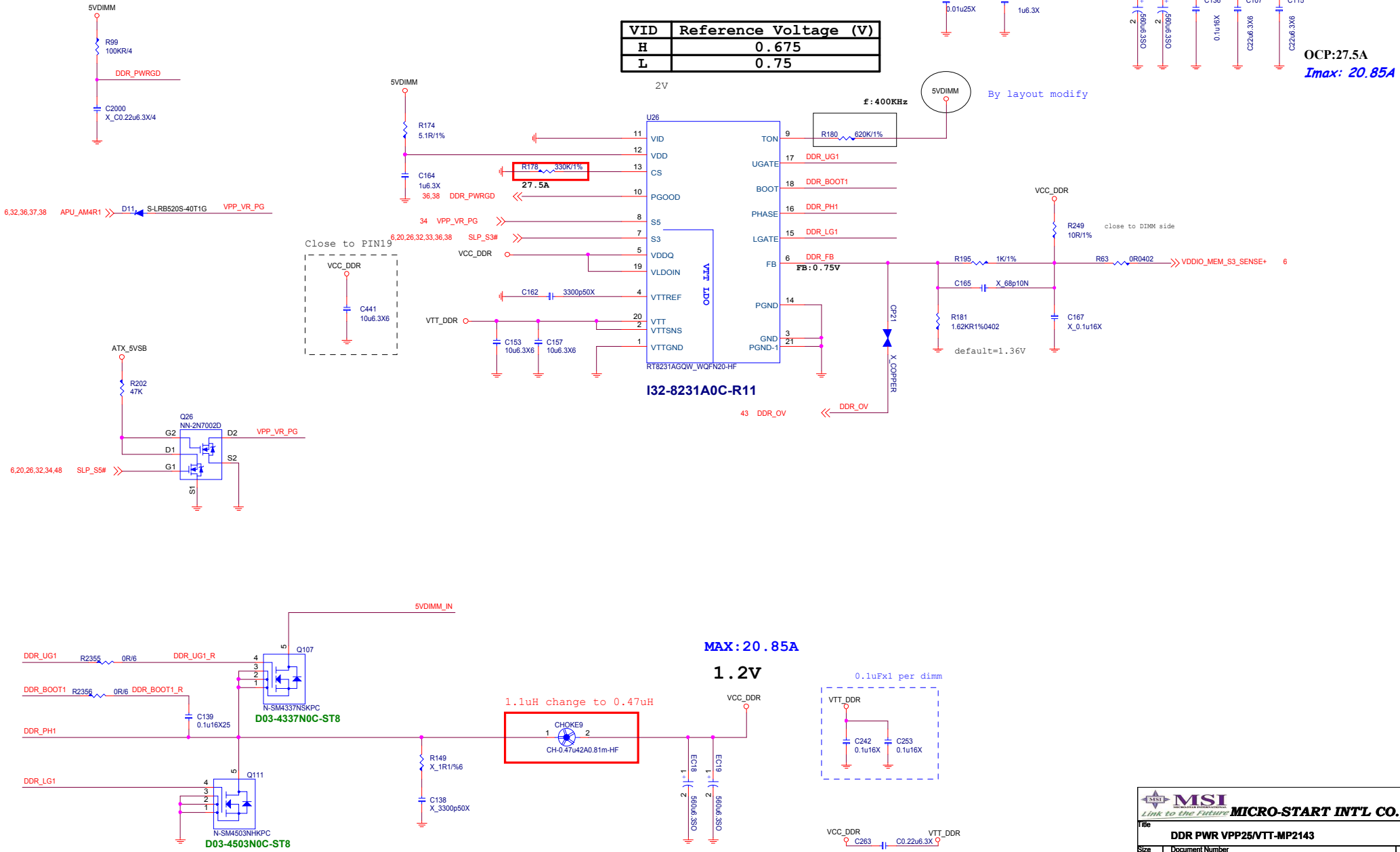


DDR4\_1.2V 15.5A+4.75A+0.6A=20.85A  
15.5A FOR CPU  
4.75A FOR 2DIMM  
0.6A FOR DDR VTT

$I_{rms} = I_{out} * \sqrt{D/N - (D)^2}$   
VCCDDR:  
 $D = V_{out}/V_{in} = 1.2/5 = 0.24$   
 $N = \text{Phase number} = 1$   
 $= 20.85A * \sqrt{0.24 - 0.0576}$   
 $= 5.21A$

VID	Reference Voltage (V)
H	0.675
L	0.75

OCP:27.5A  
I<sub>max</sub>: 20.85A



FOR CPU 1.8V S5

0.5A

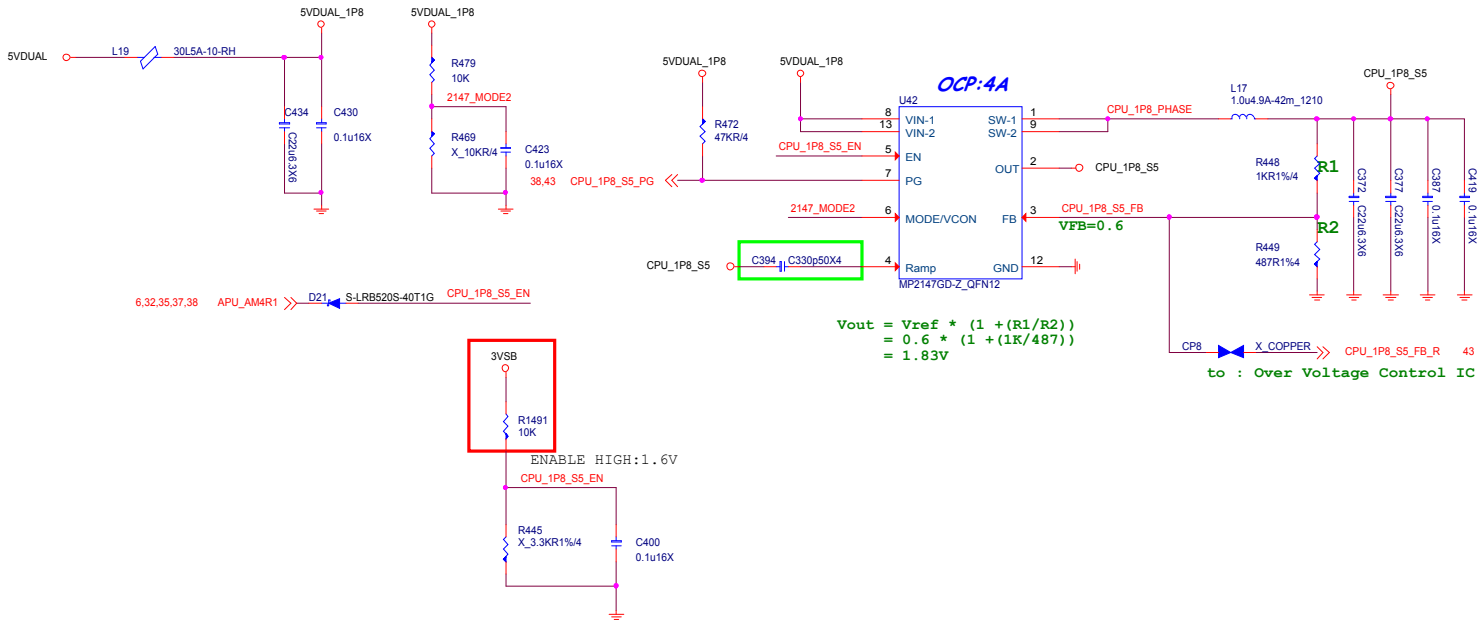
FOR VCCP\_SOC\_S5

0.9A

FOR CPU 1.8V S0

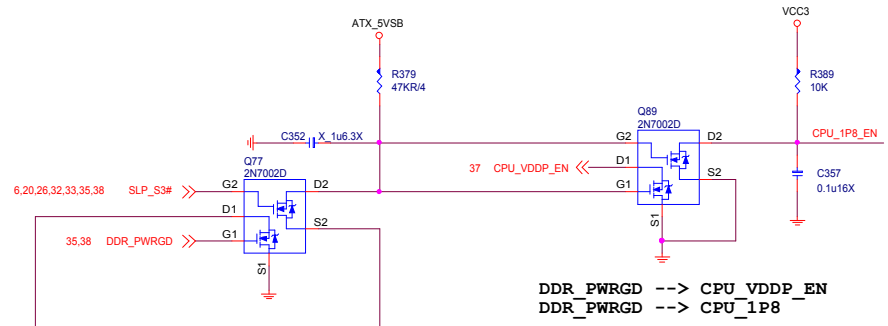
2.0A

0.5A + 2.0A + 0.9A = 3.4A



$$V_{out} = V_{ref} * (1 + (R1/R2))$$
$$= 0.6 * (1 + (1K/487))$$
$$= 1.83V$$

to : Over Voltage Control IC



ENABLE HIGH:1.7V

$$I_{limit} = (1/R_{limit}) * S, S=80000, \text{when } VIN=1.8V$$
$$= (1/16) * 80000 = 5.0375A$$
$$T_{ss} = (1/3) * ((V_{out} * C_{ss}) / I_{ss}), I_{ss}=9\mu A$$
$$T_{ss} = (1/3) * ((1.8 * 15n) / 9\mu A) = 1mS$$

DDR\_PWRGD --> CPU\_VDDP\_EN  
DDR\_PWRGD --> CPU\_1P8

# CPU\_VDDP\_S0

1.05V/0.9V@S0:8.5A

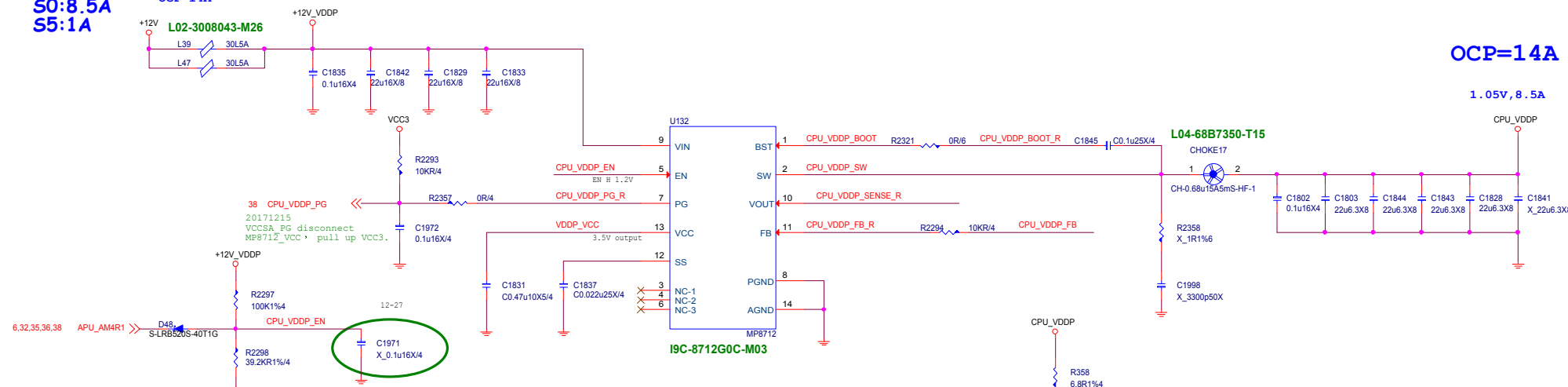
S0:8.5A  
S5:1A

OCP=14A

Input Current= (8.5A\*1.05V)/12V/0.8=0.93A

OCP=14A

1.05V, 8.5A



TYPE0\_CPU\_SEL:  
0:TYPE 0  
1:TYPE 2

TYPE1\_CPU\_SEL:  
0:TYPE 0  
1:TYPE 2

CPU\_VDDP\_EN:  
0:TYPE 2  
1:TYPE 0

Q340 2N7002D

D1 D2

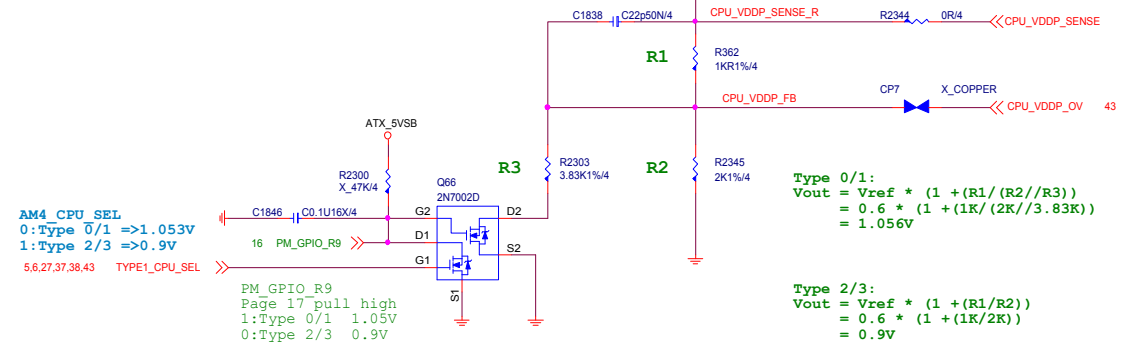
S1 S2

6,7,38 TYPE0\_CPU\_SEL

5,6,27,37,38,43 TYPE1\_CPU\_SEL

CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	1
NA	2	0	0	0
SR	2	1	1	0
RV/ZP	3	0	1	1

**CPU VDDP NOT SUPPORT TYPE2**



Type 0/1:  
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$   
 $= 0.6 * (1 + (1K/(2K//3.83K)))$   
 $= 1.056V$

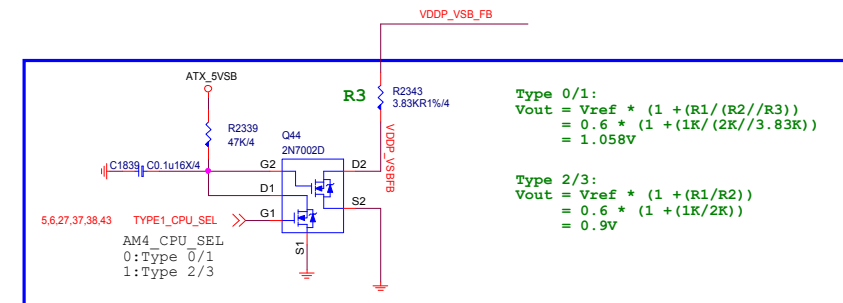
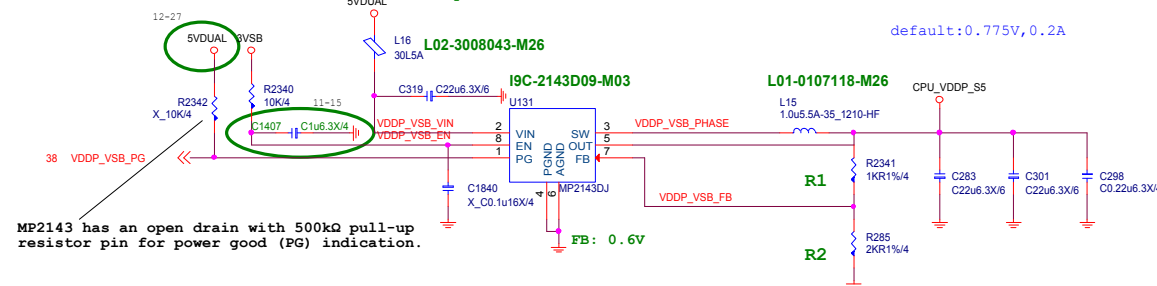
Type 2/3:  
 $V_{out} = V_{ref} * (1 + (R1/R2))$   
 $= 0.6 * (1 + (1K/2K))$   
 $= 0.9V$

# CPU\_VDDP\_S5

1.05V/0.9V  
S5:1A

Input Current=0.04A

default:0.775V,0.2A

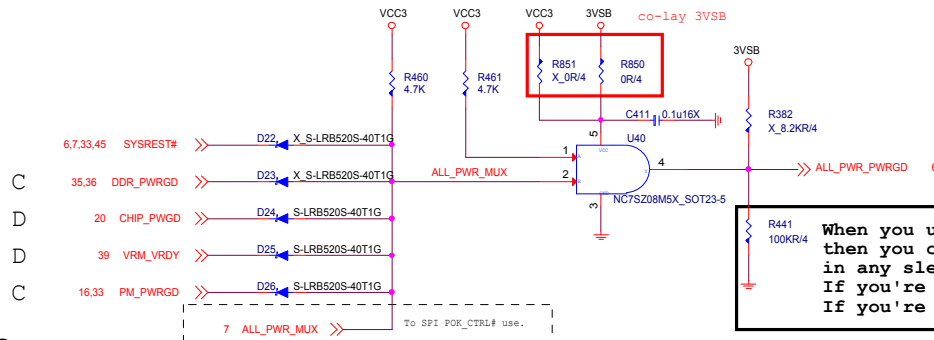


Type 0/1:  
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$   
 $= 0.6 * (1 + (1K/(2K//3.83K)))$   
 $= 1.058V$

Type 2/3:  
 $V_{out} = V_{ref} * (1 + (R1/R2))$   
 $= 0.6 * (1 + (1K/2K))$   
 $= 0.9V$

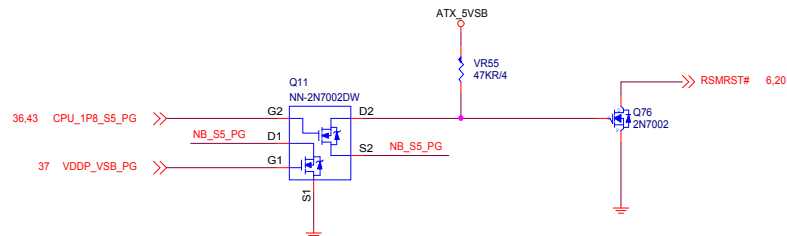
MP2143 has an open drain with 500kΩ pull-up resistor pin for power good (PG) indication.

## ALL POWER GOOD MUX

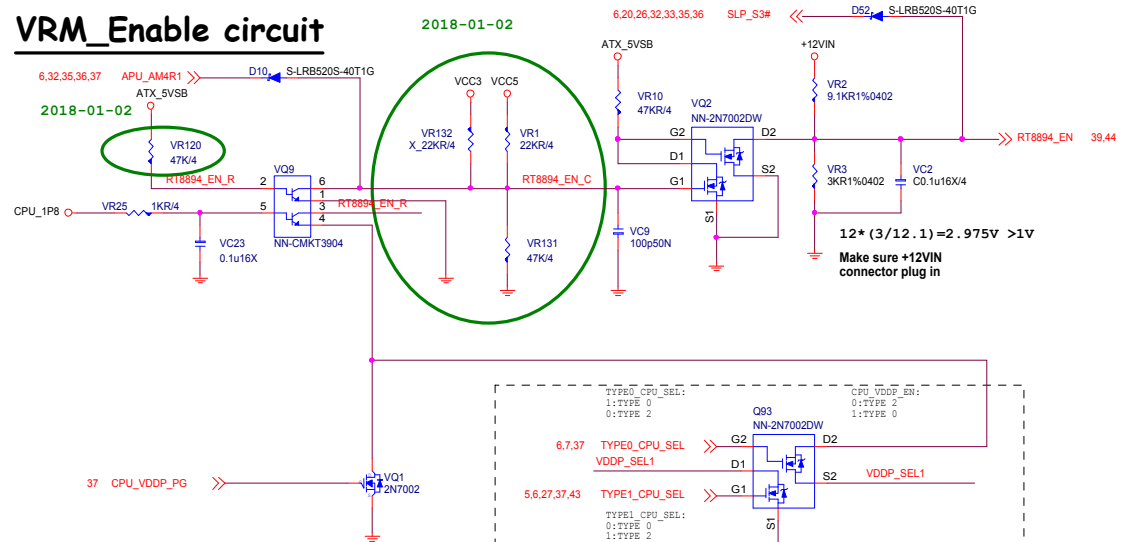


S0 PG

S5 PG



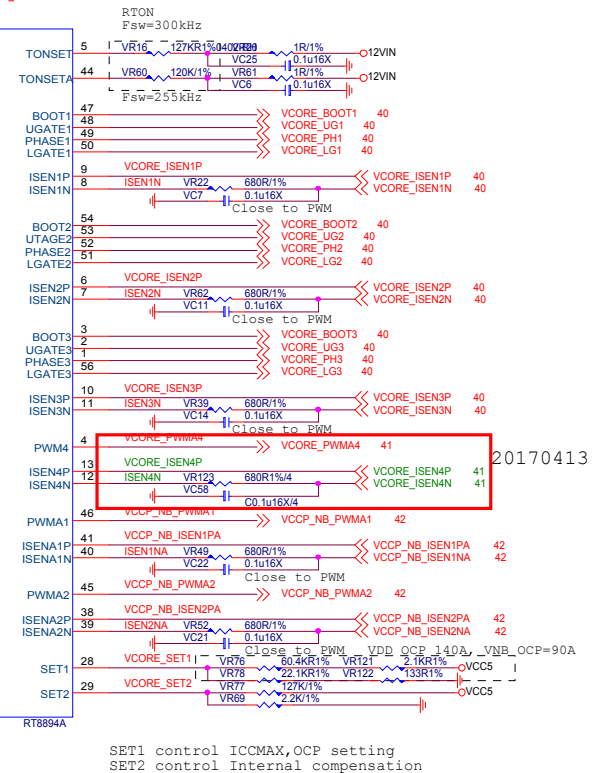
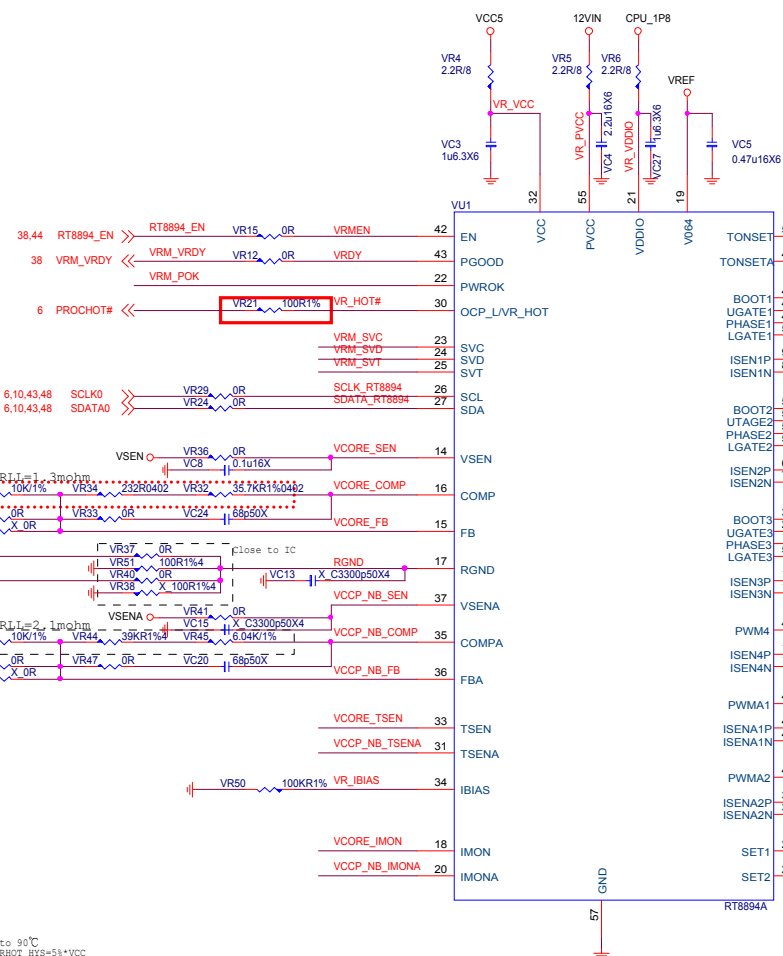
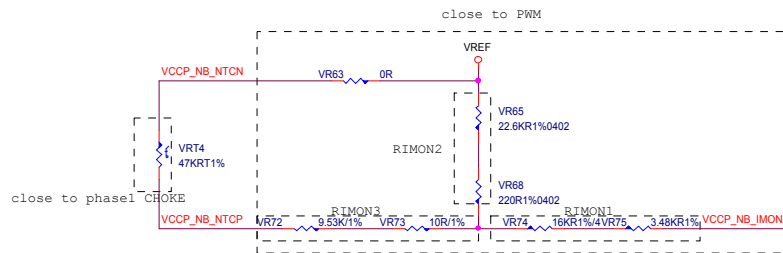
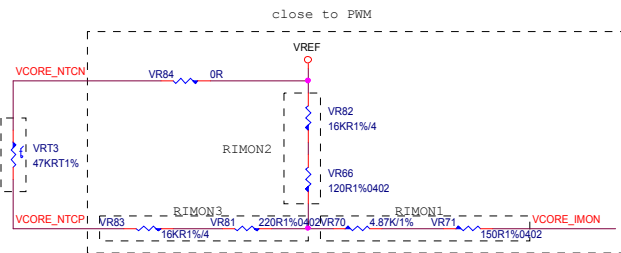
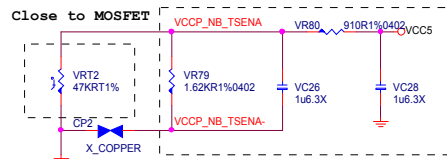
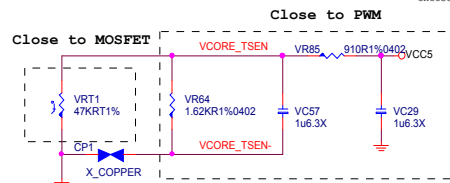
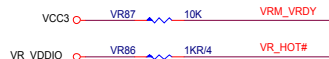
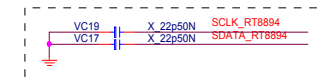
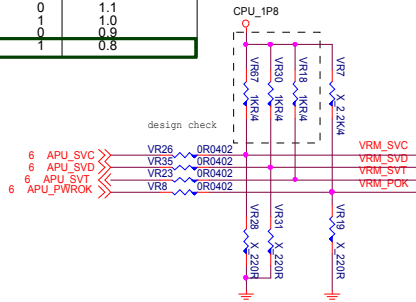
## VRM\_Enable circuit



CPU VDDP NOT SUPPORT TYPE2

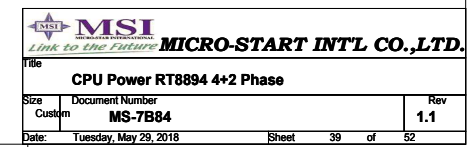
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	0	0	0
SR	2	1	1
RV/ZP	3	1	0

		BOOT VOLTAGE
SVC	SVD	Pre PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

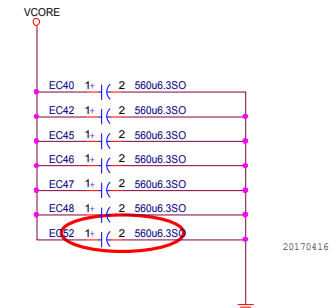
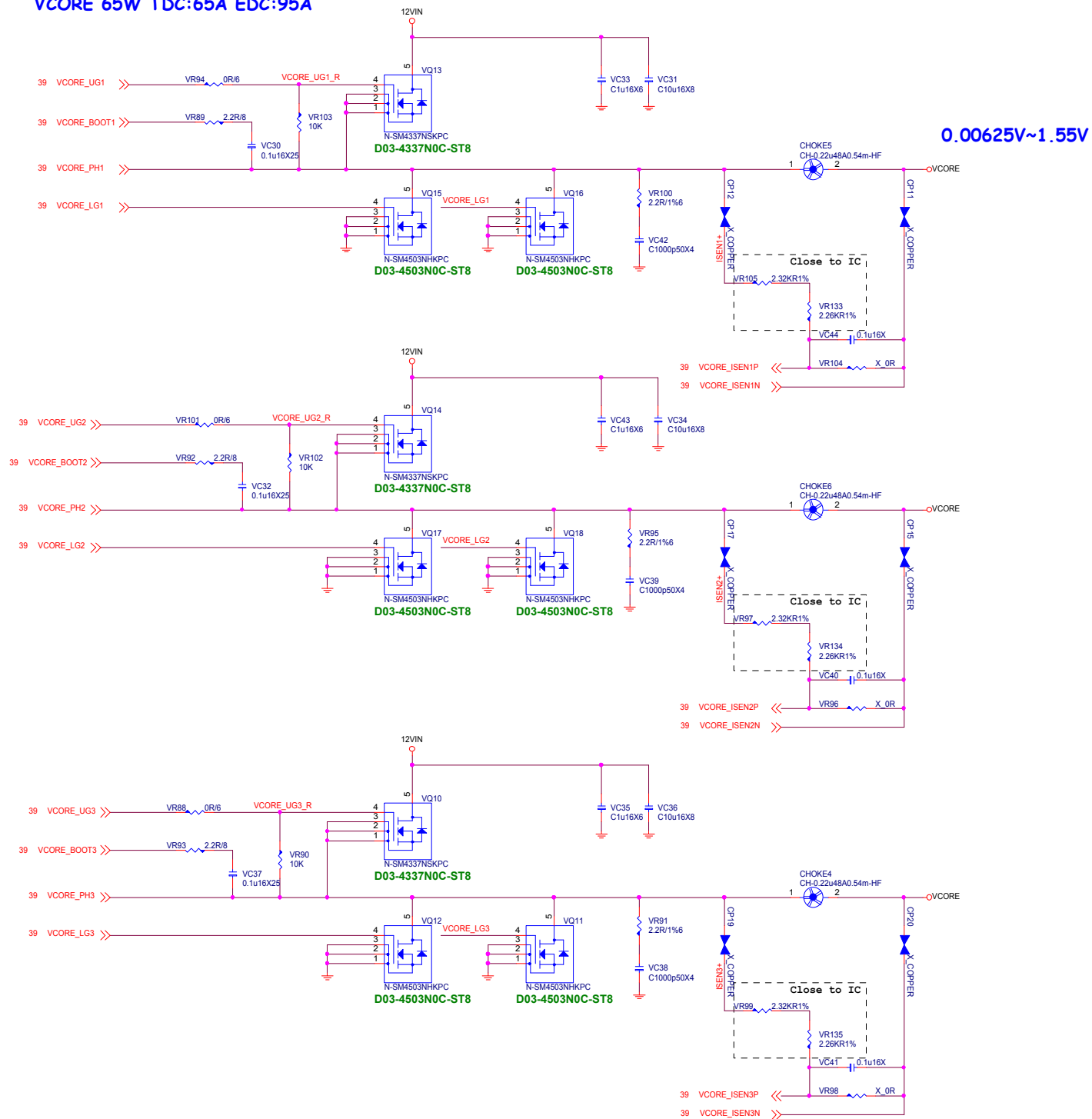


VCORE IccMAX: 125A =>OCP=>140A  
VCC NB IccMAX: 75A =>OCP=> 90A

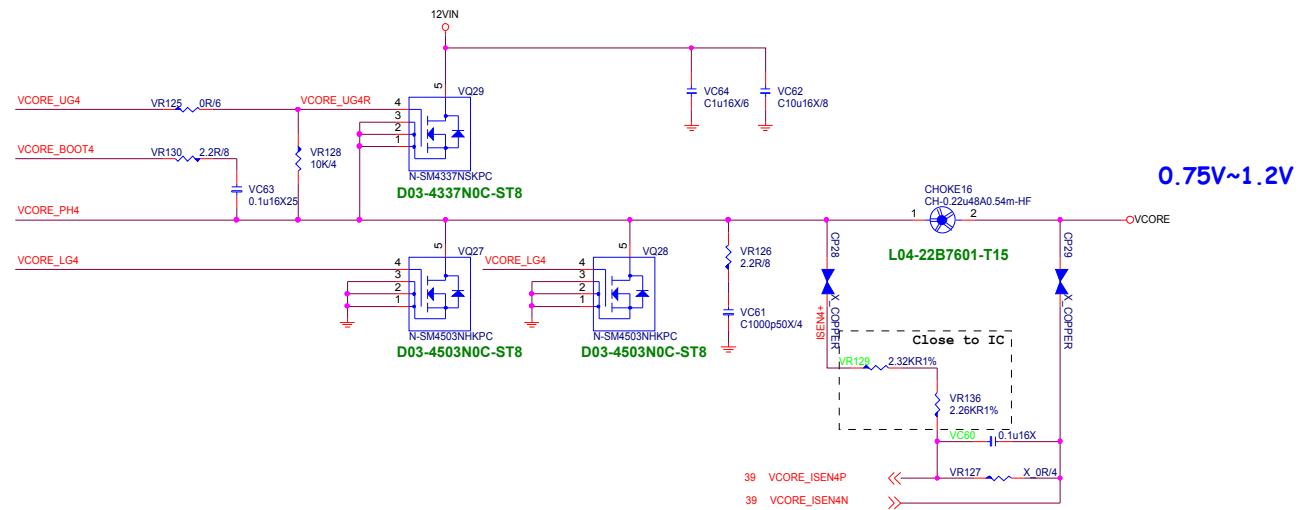
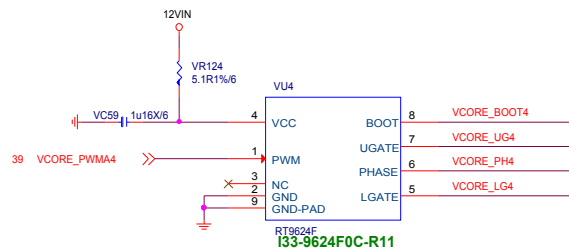
SMB Address: 0X40



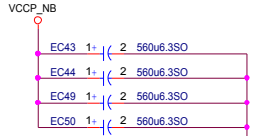
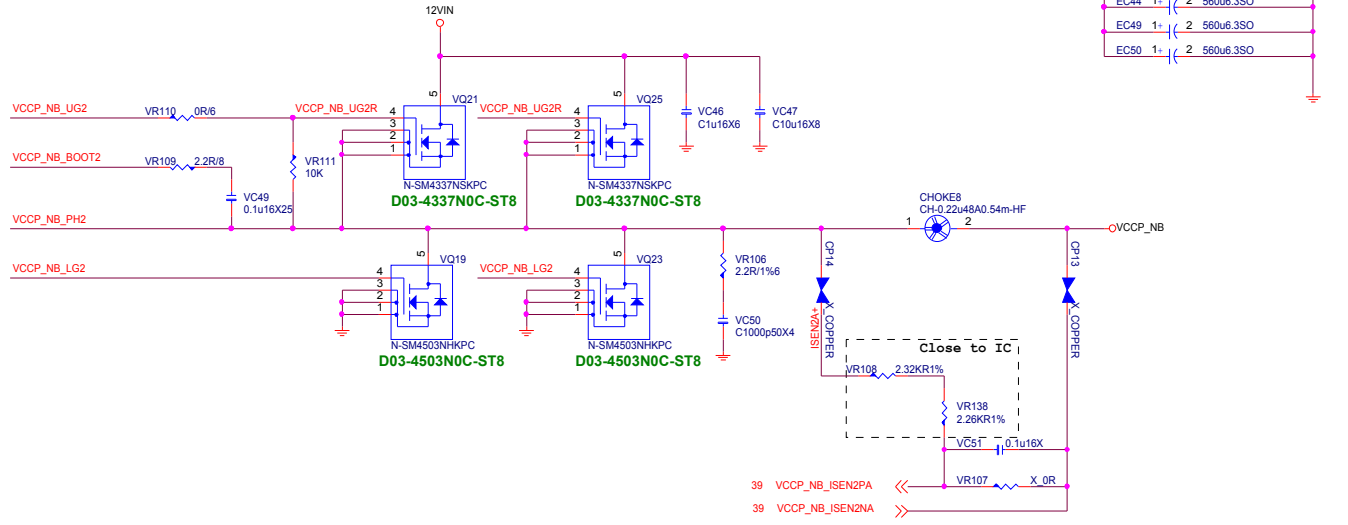
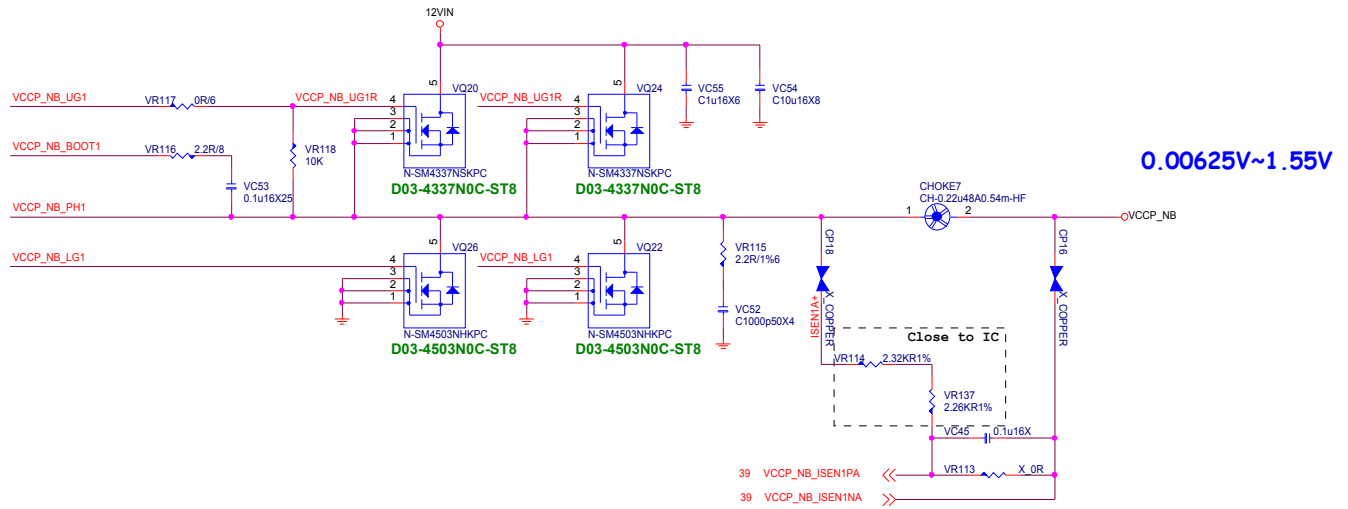
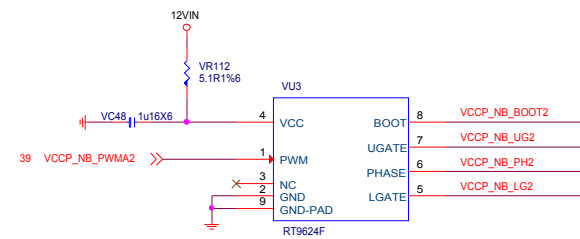
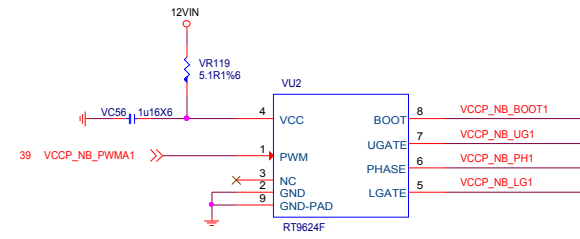
VCORE 95W TDC:80A EDC:125A  
VCORE 65W TDC:65A EDC:95A







VCCP\_NB 95W TDC:50A EDC:75A  
VCCP\_NB 65W TDC:50A EDC:75A



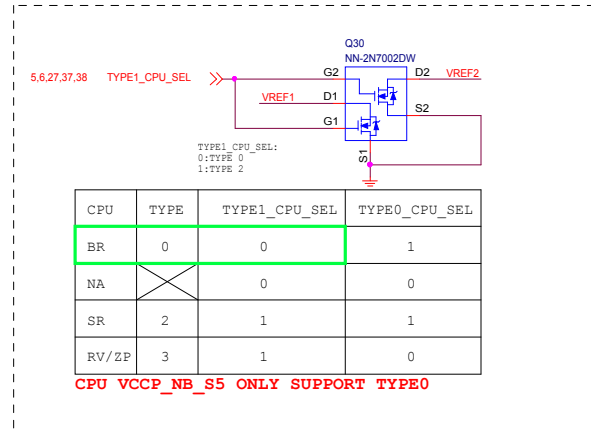
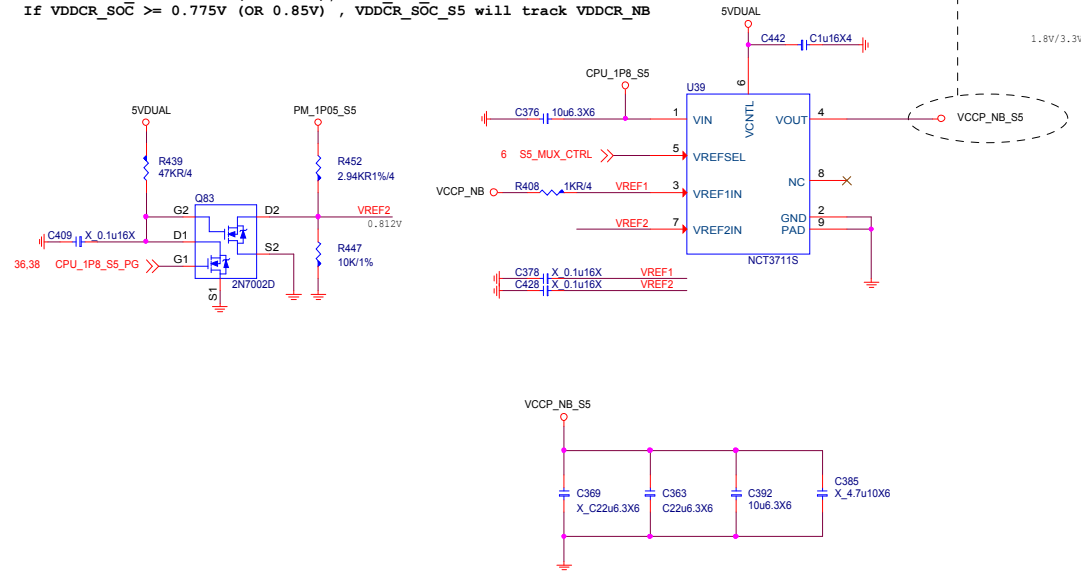
FOR  
VCCP\_SOC\_S5  
0.9A

(VDDCR\_SOC\_S5 is only used for AMD TYPE0)

TYPE0 Only

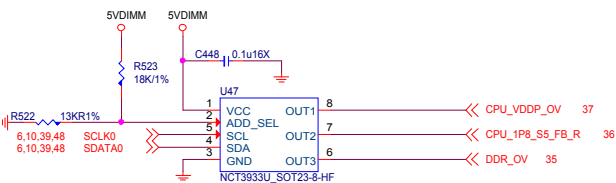
S5\_MUX\_CTRL  
HIGH:S0  
LOW: S3/S5

H: +VDDCR\_FCH\_ALW will track VDDNB  
L: If VDDCR\_SOC<0.775V (OR 0.85V), VDDCR\_SOC\_S5 =0.775V.  
If VDDCR\_SOC >= 0.775V (OR 0.85V), VDDCR\_SOC\_S5 will track VDDCR\_NB

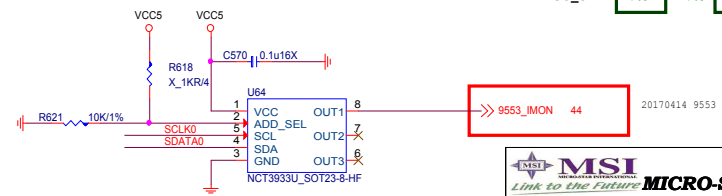


## Over Voltage Control IC

0x26: RH=18K, RL=13K



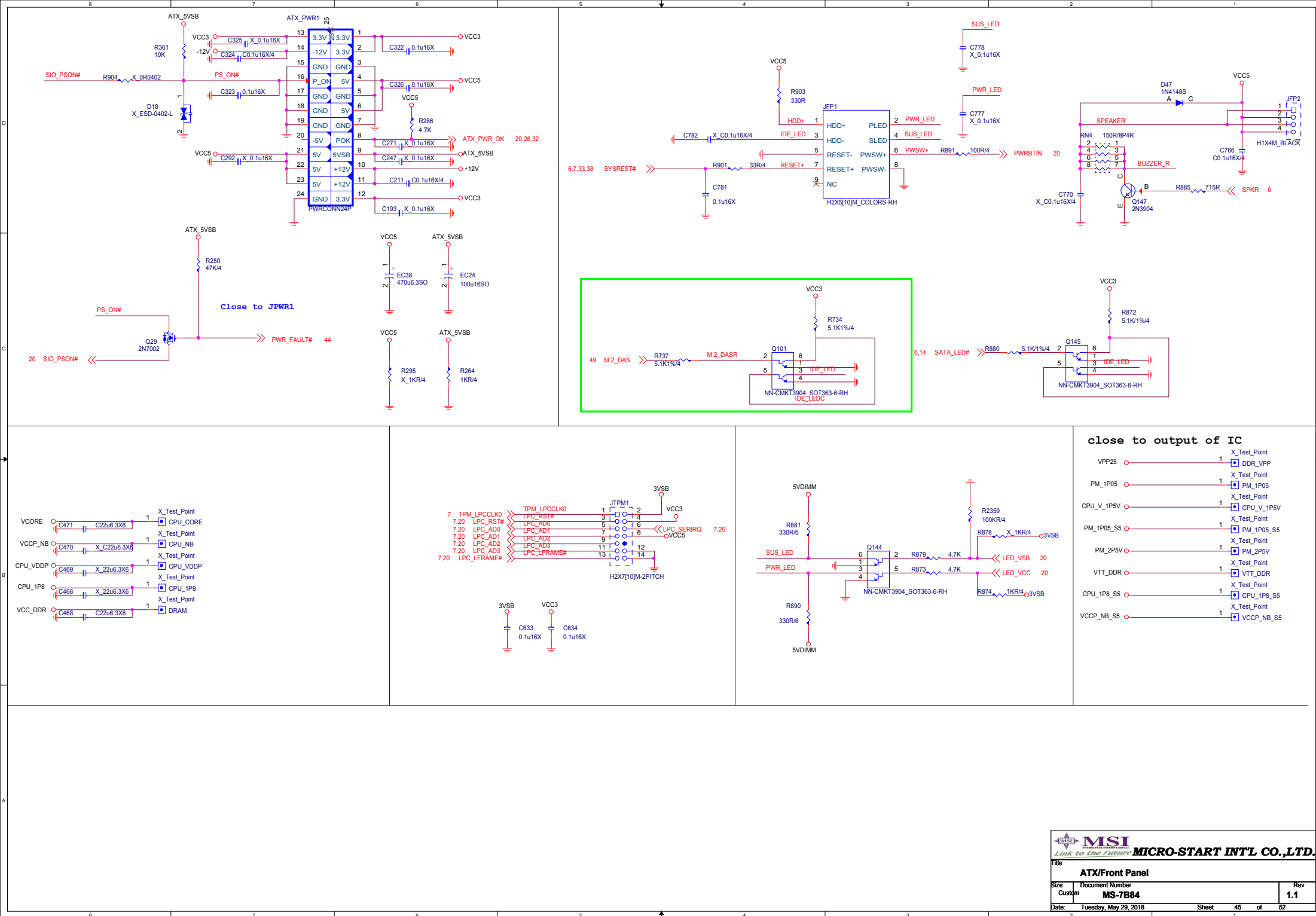
0x2A: RH=OPEN, RL=10K



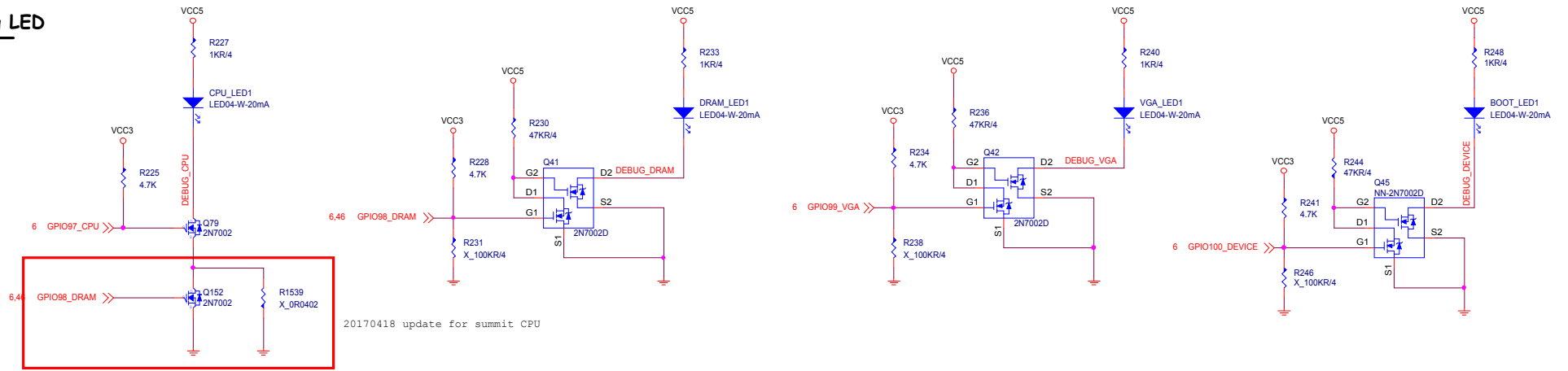
## UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%





## EZ Debug LED

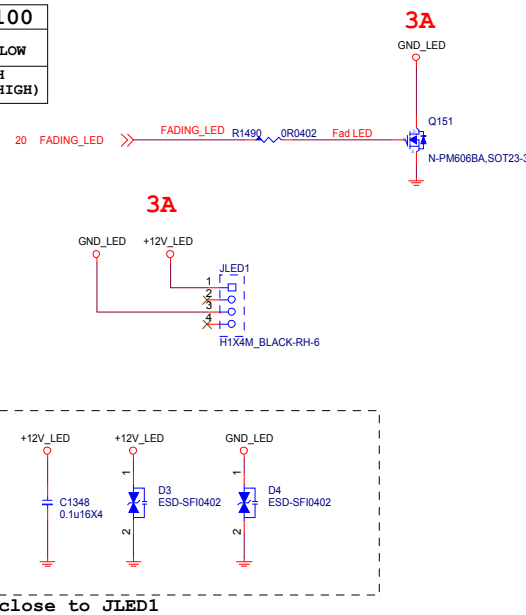
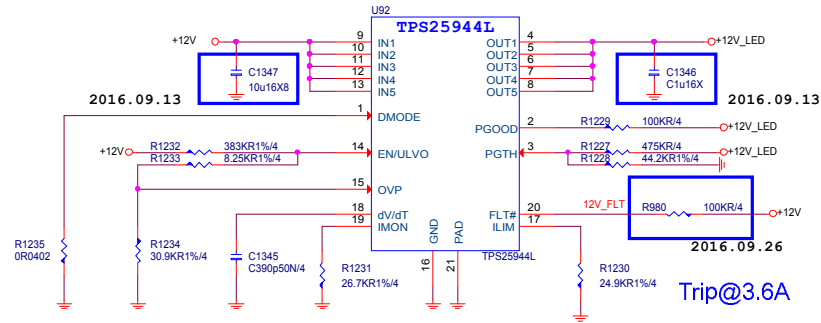


## LED Control by SIO

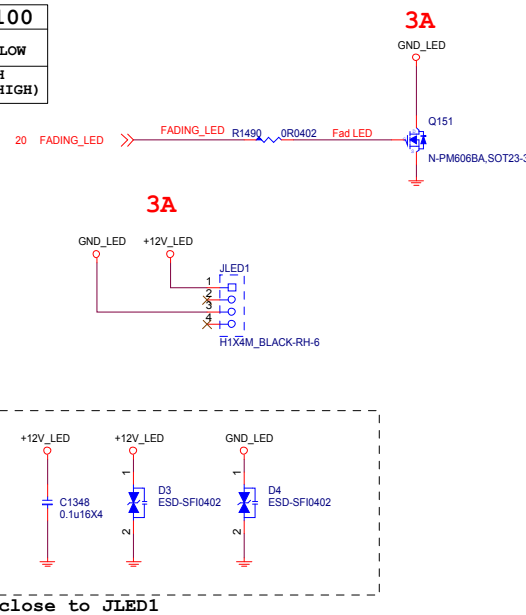
### JLED

2016.07.06 Use TPS25944L

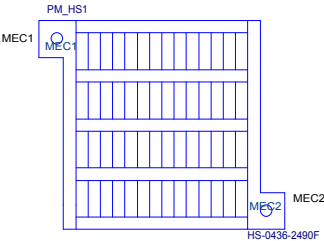
LED	GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮		GPI FULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅		GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)



## AM4 APU Detect LED Circuit



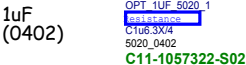
HEAT SINK



5010 Level



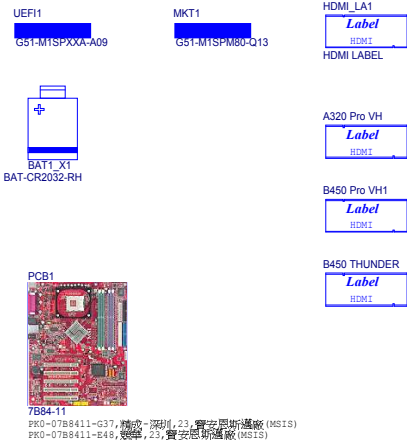
5020 Level



60 Level



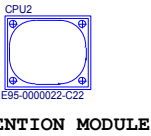
MANUAL PART



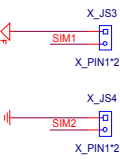
MOS HS(VCORE)

OPT	Configure	BOM	Function
		601-7B84-A01	XXXX

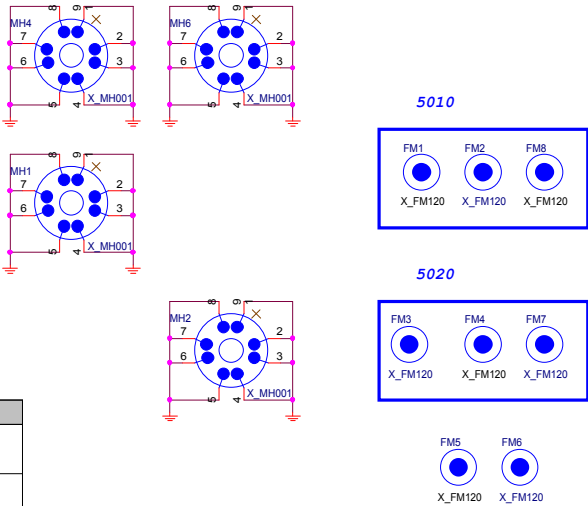
CPU Socket

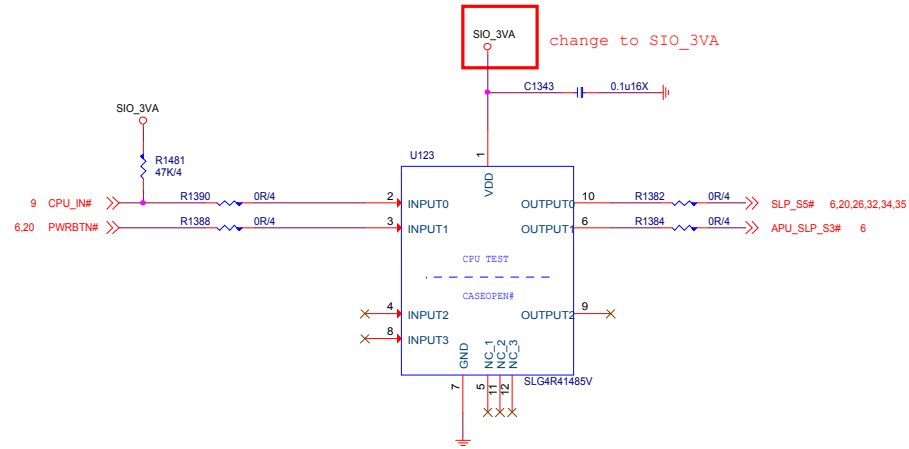


Simulation

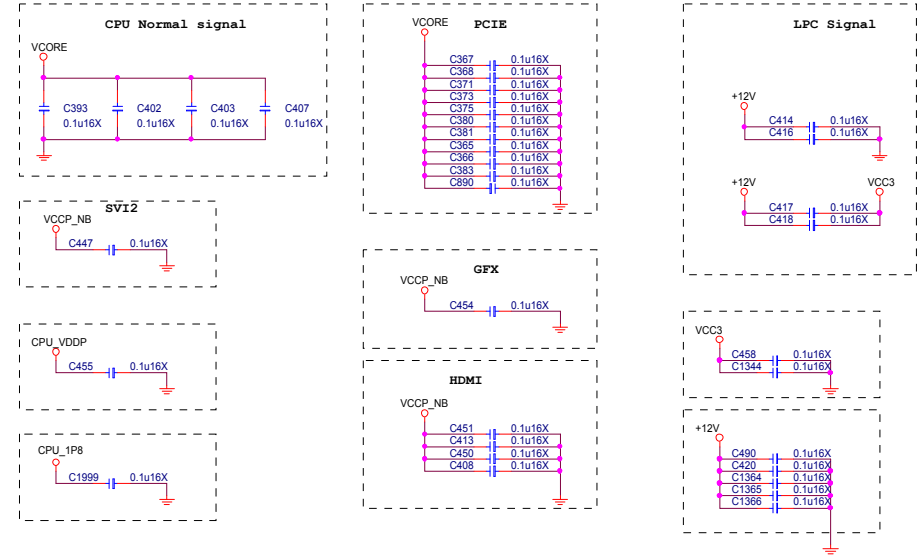


Optics Orientation Holes

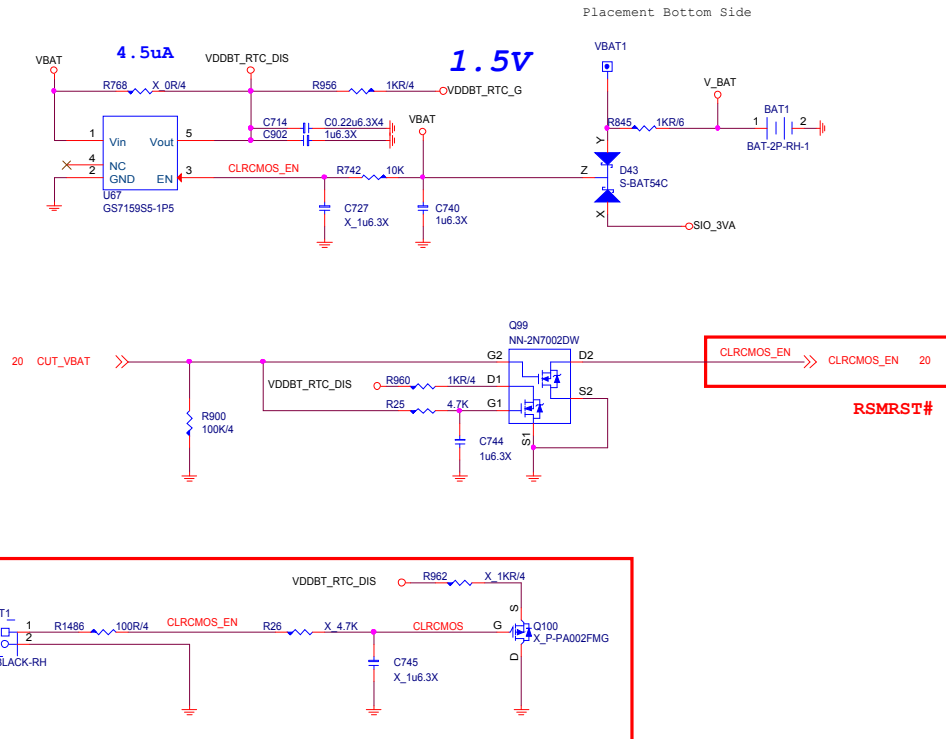




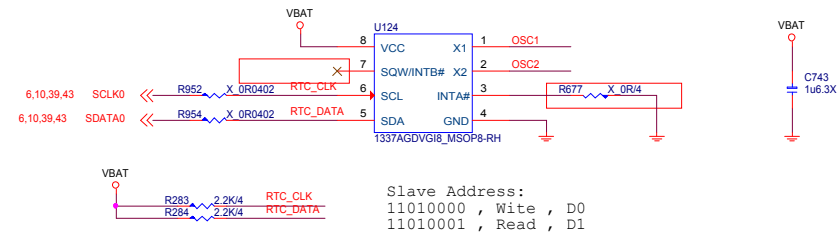
## Moat Cap



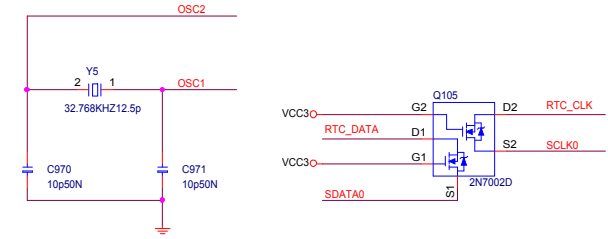
## RTC & Clear CMOS Circuit



20170413 PIN7floating PIN3 reseed pull down



Slave Address:  
11010000 , Write , D0  
11010001 , Read , D1

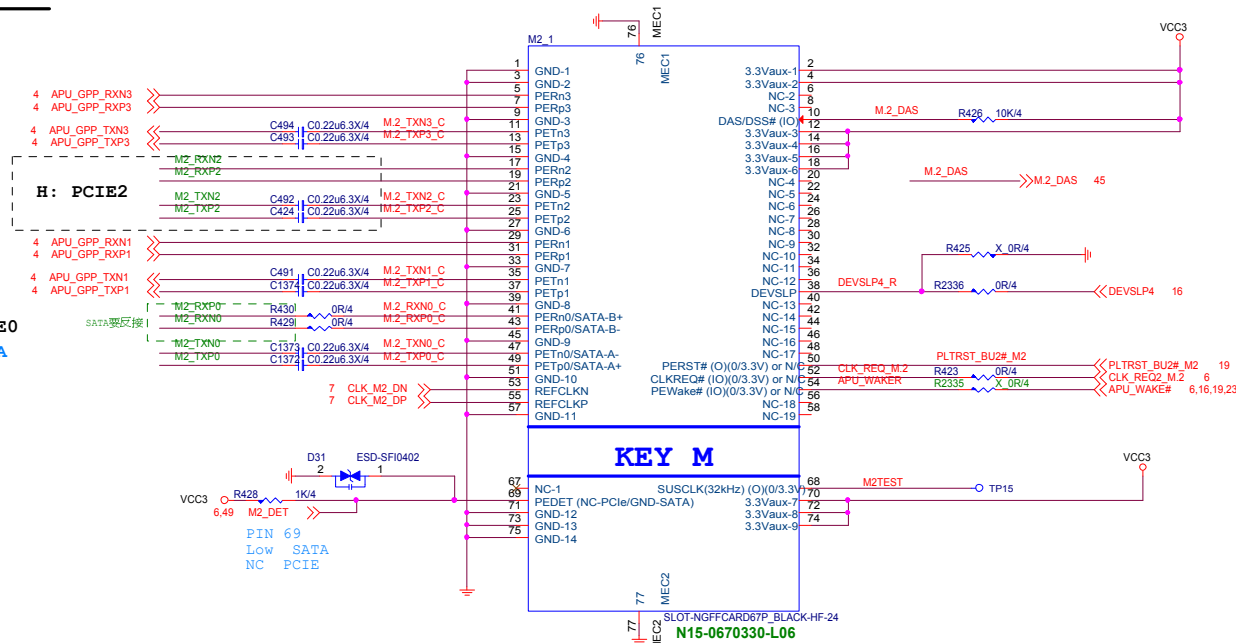




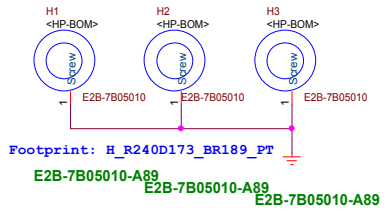
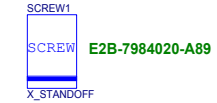
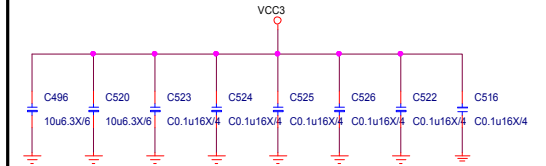
# M.2 Connector

3.3V@2.5A

H: PCIE0  
L: SATA



3.3V@2.5A



## M.2 Switch

